TEXAS INSTRUMENTS

DIGITAL

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DESIGN SEMINAR 99

REFERENCE MANUAL

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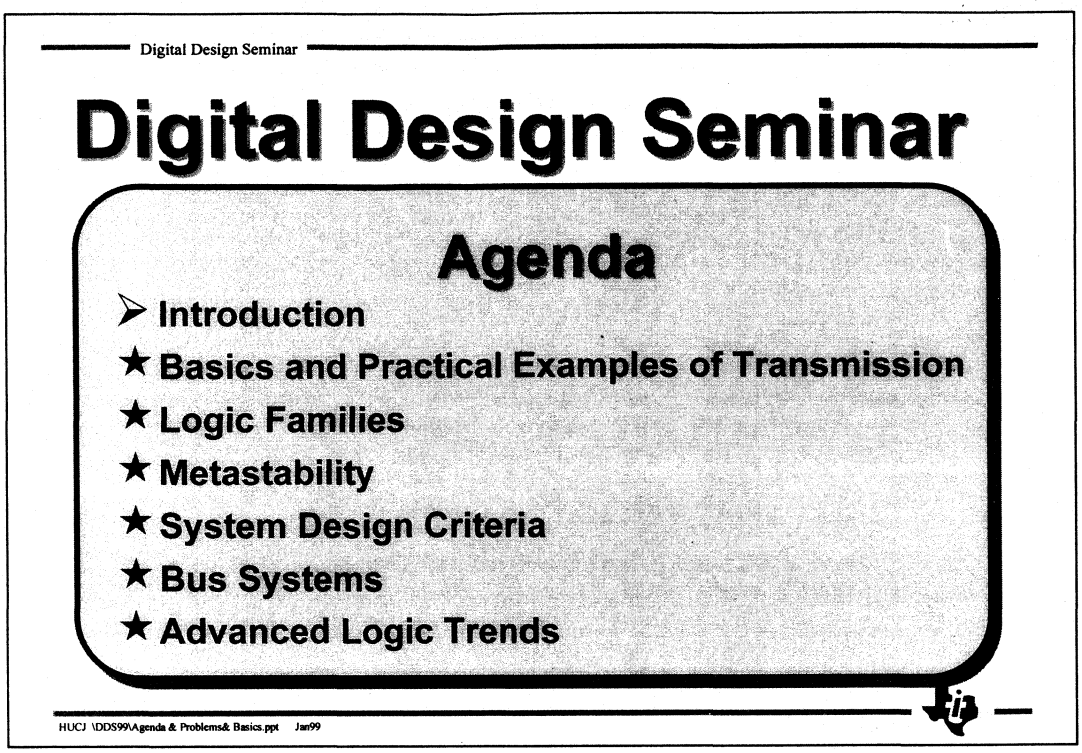
Digital Design Seminar
Digital Design Seminar
Agenda
Introduction
Basics and Practical Examples of Transmission
Logic Families
Metastability
System Design Criteria
Bus Systems
Advanced Logic Trends
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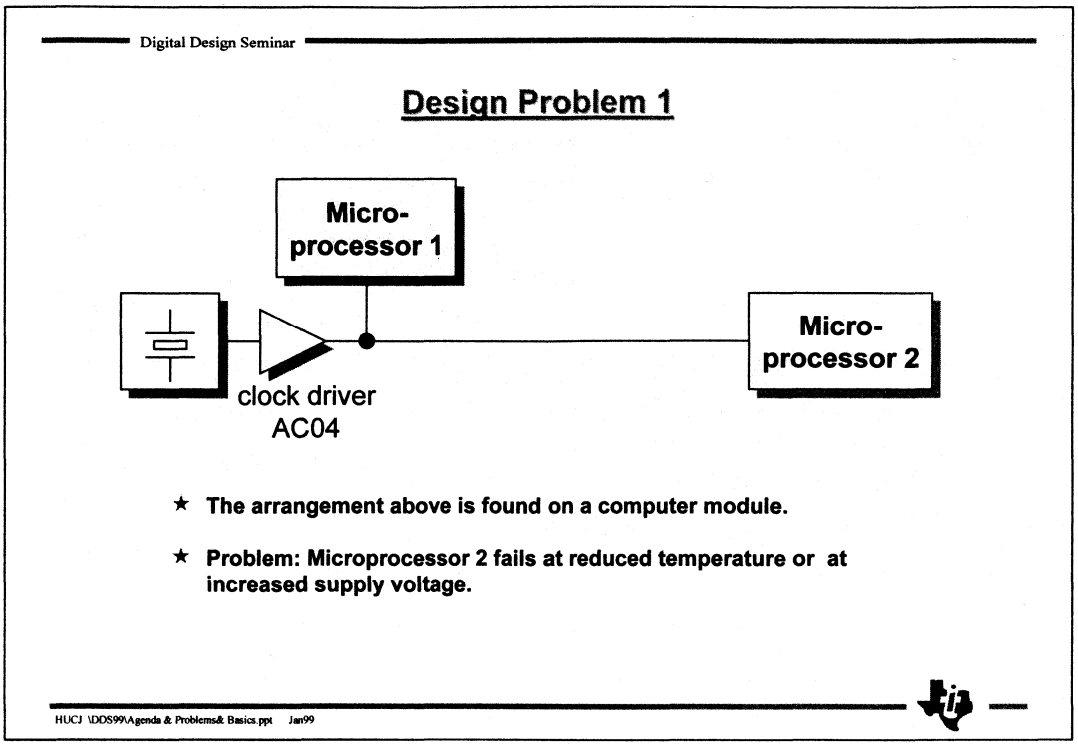


The above example shows a multi-processor system. Both processors get the same clock signal and are running synchronously. The designer builds up the system and finds that at reduced temperature or increased supply voltage Microprocessor 2 fails.

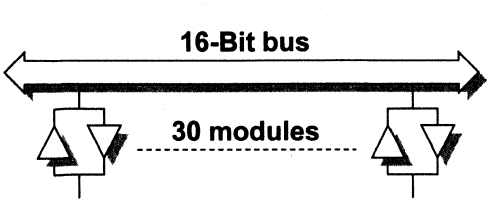
After replacing Microprocessor 2 with a new device, the system still fails. Processor 1 and 2 are exchanged; now Processor 1 fails in socket 2, while Processor 2 works perfectly in socket 1.

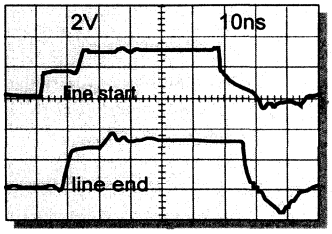
Obviously there is a problem with socket 2, but the designer doesn't know what to do.

At the end of the section "Bus Systems", the solution of this problem is found.

Digital Design Seminar

Design Problem 2





★ **Signal distortion limits the data rate to 20 MByte/s (10 Mbit/line).**

★ **Transmission reliability is poor.**

★ **System power dissipation is extremely high**

2 x F245 transmitting	I_{CC} = 200 mA
2 x F245 receiving	I_{CC} = 200 mA
56 x F245 3-State	I_{CC} = 6160 mA
total	I_{CC} = 6560 mA

★ **Use of Advanced CMOS reduces the power dissipation, but worsens signal distortion.**

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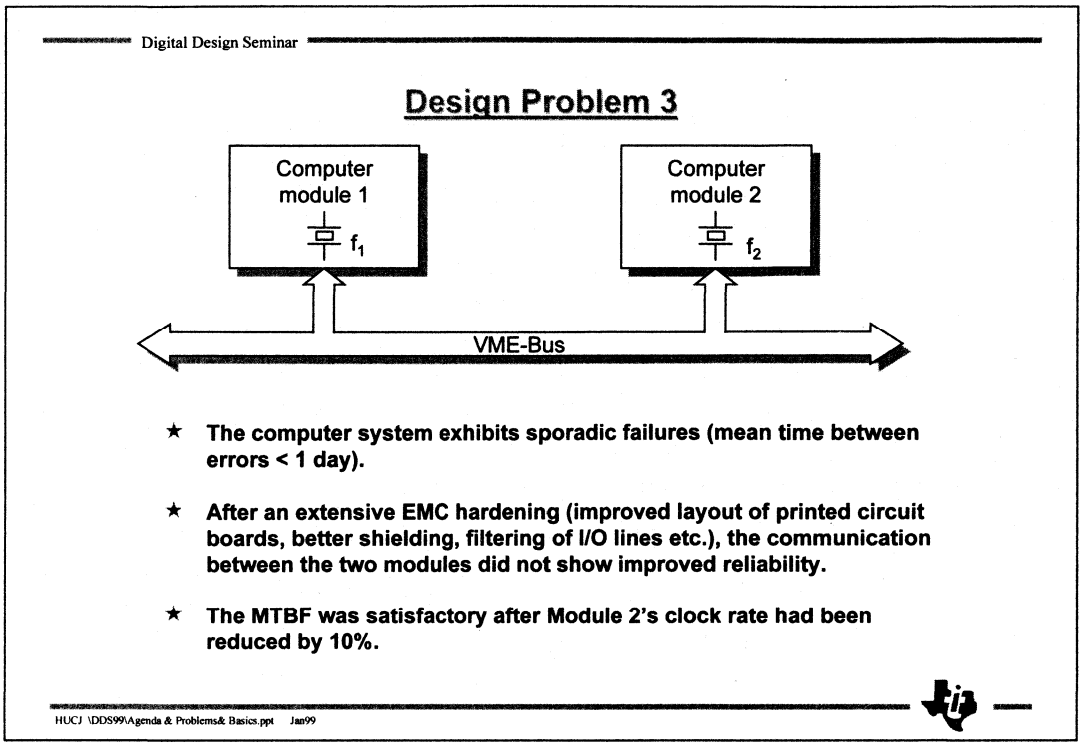
A 16-bit backplane bus with 30 modules plugged into it has to be developed. Because the designer was successful in using F245 transceivers in the past, these circuits are chosen to drive the backplane.

A gance at the waveforms on this bus with a oscilloscope shows bad signal quality. At the driver output, stairs in the rising edge are observed and at the end of each signal trace there is an undershoot in the range of -1.5V. On the other hand the 60 bus-transceiver has a huge power-consumption. A theoretical calculation shows a worse case supply current of 6.5A for the bus functions only.

The aim is to reduce the power consumption and improve the signal quality. The first idea is to use CMOS circuits, well known for their low power consumption. Replacing the F245 transceiver with AC245 devices reduces power consumption, but the signal quality becomes even worse. The designer had no idea how to improve the bus-system at this point.

To see the solution of this problem, please look at the end of the section “Bus Systems”.

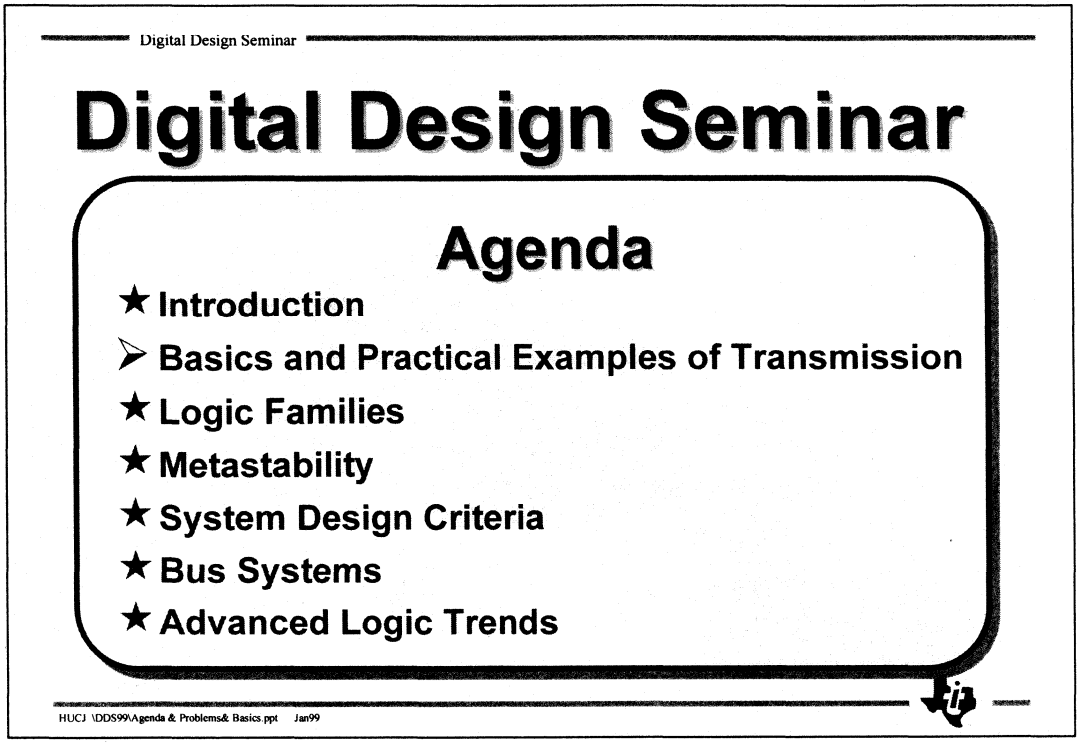


A multiprocessor system, connected through the VME-bus, was designed and running well. After 12 hours, processor module 2 fails; a system reset solves the problem. But again after a further 14 hours, processor module 2 fails again.

Now the designer made a lot of improvements regarding EMC-behaviour, thinking EMC to be the root cause of the problem (introduction of a main-line-filter, new board layout, new metal cabinet, etc. But the improvement was negligible.

Now the designer was desperate and tried this and that. During these experiments he found out that a reduction of f_2 by 10% seemed to solve the problem. But the system requirement was 100% f_2 and not 90% f_2 and so the root cause of failure still needed to be found.

The solution of this problem can be found at the end of the section "Bus Systems".


Digital Design Seminar
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★ Introduction
➢ Basics and Practical Examples of Transmission
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★ Metastability
★ System Design Criteria
★ Bus Systems
★ Advanced Logic Trends
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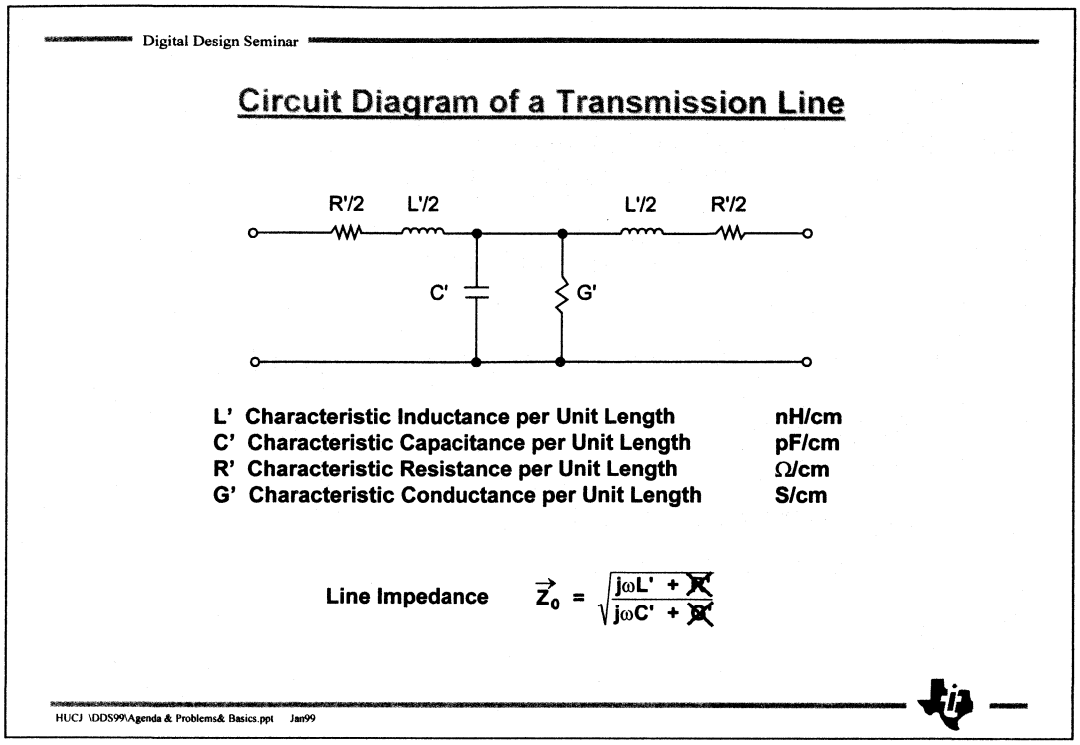


Circuit diagram of a Transmission Line

The equivalent circuit of a transmission line consists of an inductance L' representing the inductance of the transmission line, a resistor R' representing the ohmic resistance of the line, a capacitance C' representing the capacitance of the line and the conductance G' representing the losses in the capacitance of the line. All these values are length dependent and are therefore specified in unit/length, e.g.: nH/cm, pF/cm, Ω/cm, and S/cm. By setting up differential equations, one can calculate the impedance of a transmission line:

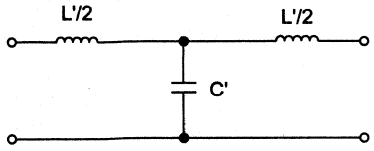
$$\underline{Z}_0 = \sqrt{\frac{j\omega L' + R'}{j\omega C' + G'}}$$

In practice this equation is difficult to handle. First, the line impedance results in a complex number which makes the required calculations time consuming. Second the line impedance is frequency dependent. This becomes uncomfortable in digital circuits, where one has to consider many frequencies simultaneously.

Digital Design Seminar

Loss-free Transmission Lines

At high frequencies the transmission line losses on printed circuit boards in digital systems can be neglected.



With R' << jωL' and G' << jωC':

Line impedance	$Z_0 = \sqrt{\frac{L'}{C'}}$	**(real number !)**
Propagation time	$\tau = \sqrt{L' \times C'}$	
Cut-off-frequency	$f_0 = \frac{1}{2\pi\sqrt{L' \times C'}}$	**with L',C' → 0 ⇒ $f_O = \infty$**

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Loss-Free Transmission Lines

In digital circuits low frequencies are not generally of concern. At higher frequencies (above some 10 kHz) the impedance of the inductance jωL' becomes large compared to the resistance R' of the wire. The admittance jωC' is also much greater than the corresponding conductance G'. Under this assumption R' and G' can be neglected. The impedance of the transmission line can now be calculated by the simple formula

$$Z_O = \sqrt{\frac{L'}{C'}}$$

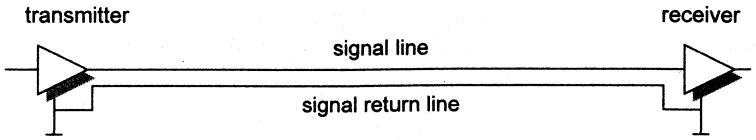
The impedance is now a real number which can be handled like an ohmic resistor. A further advantage is Z_0 is now independent of the frequency.

An important parameter in data transmission circuits is the propagation time t_p of the signal on a transmission line. This time is also determined by the parameters of the line:

$$t_p = \sqrt{L' \cdot C'}$$

On typical cables used in transmission circuits (coaxial cable, twisted pair cable) the propagation time becomes t_p = 5 ns/m. This reflects a propagation speed v = 200 000 km/s (about 60 % of the speed of light).

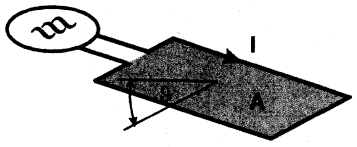
Transmission Line



A transmission line consists of
- a signal line, which carries the signal current
- a signal return line (mostly GND) which carries a return current of the same magnitude.

Any DC interconnect between the GND terminals of the two circuits(e.g. safety earth) will not provide a signal return path according to transmission line theory.

The area between the signal line and the return lines determines the capability of the circuit to radiate RF and also its susceptibility to EMI.



$$E = k \times I \times A \frac{1}{r} \times \sin \vartheta$$

Transmission Line

The designer has to keep in mind that a transmission system always has two conductors: the signal line and the signal return line. Both lines have to be designed carefully to ensure the required quality of the interface circuit. A random signal return path (e.g. via the protective ground wire) is not an adequate signal return line.

Both wires - the signal wire and the signal return wire - act as an antenna which influences the electromagnetic compatibility of the interface circuit. The larger the area between these wires, the larger will be the probability that electromagnetic energy is radiated, which may affect neighbouring equipment. Similarly the area between these wires also determines the electromagnetic susceptibility of the interface circuit.

Transmission Line Theory

Rule of Thumb:
Transmission line theory has to be applied, when the rise time of the signal is shorter than twice the propagation time.

Example 1 : Twisted pair cable; τ = 5 ns/m ; t_r = 2 ns

$$L = \frac{t_r}{2 \times \tau} = \frac{2\ ns}{2 \times 5\ ns/m} = 0.2\ m$$

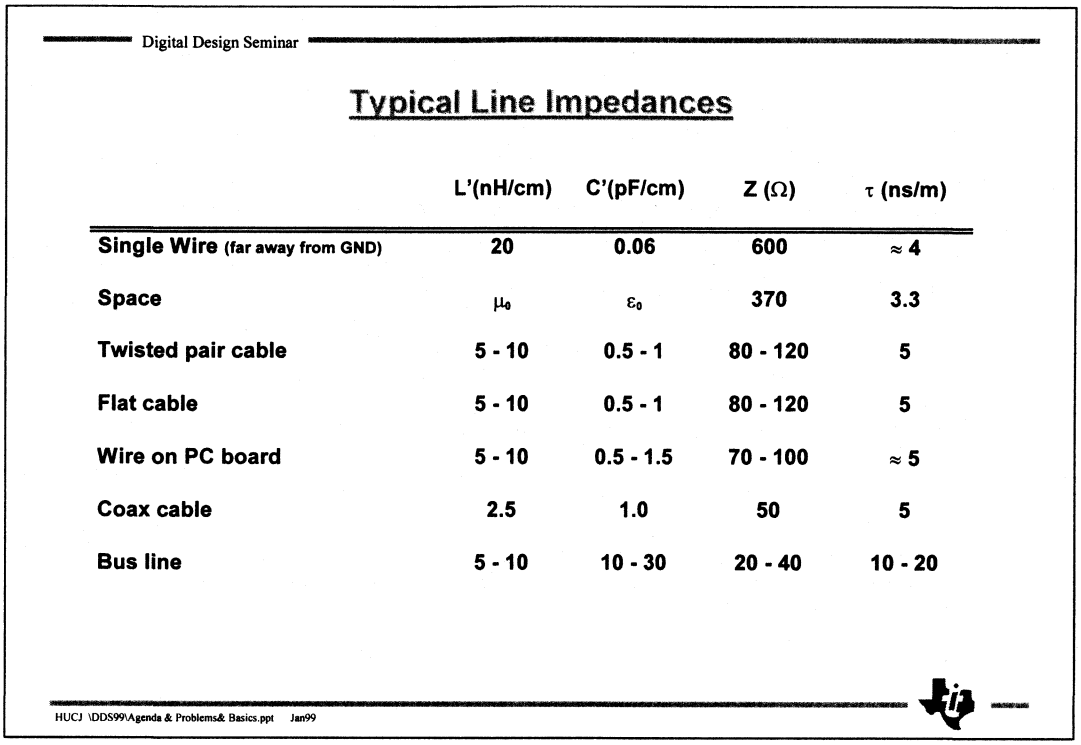
Example 2 : Bus Line; t = 20 ns/m ; tr = 2 ns

$$L = \frac{t_r}{2 \times \tau} = \frac{2\ ns}{2 \times 20\ ns/m} = 0.05\ m$$

With shorter signal lines all line reflections occur during the rise/fall time of the signal. In this case it is allowed to use the simplified capacitive load line model.

Transmission line theory

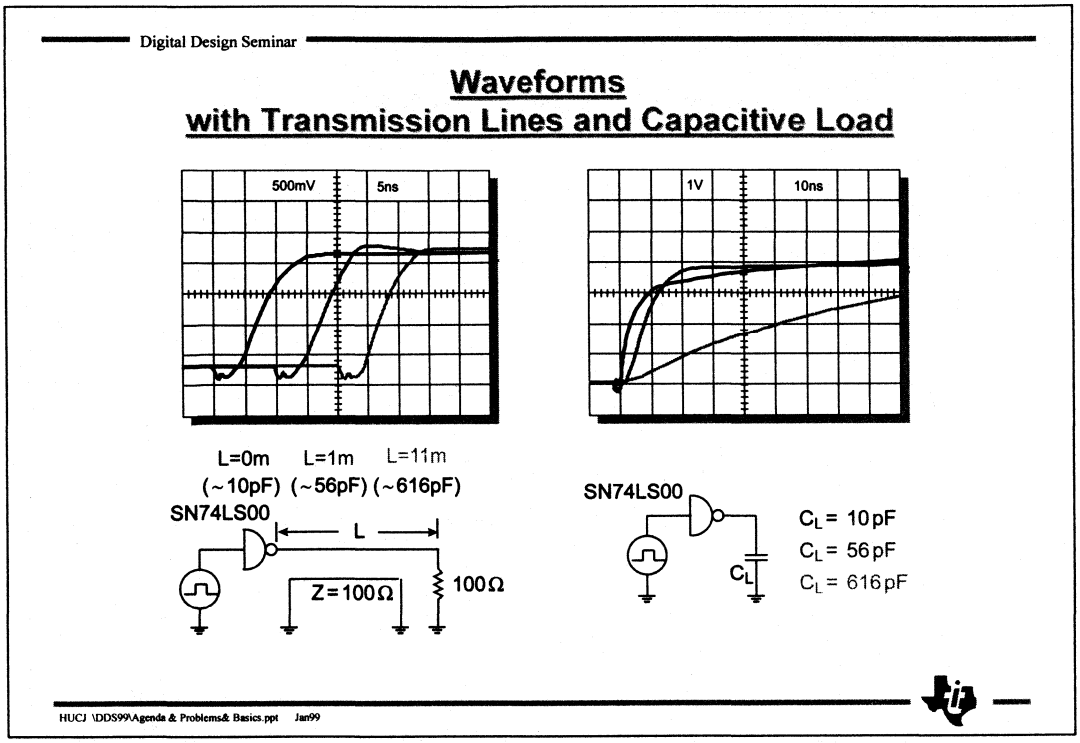
Transmission lines have to be treated as lines in accordance with transmission line theory when twice the signal propagation time becomes longer than the rise time of the signal - i.e.: when the line reflections no longer fall into the rise time interval. For a given rise time t_r = 5 ns and a typical propagation time of the signal t_p = 5ns/m, the critical line length in l_{max} = 1 m. In applications where the propagation time of the signal is much longer - e.g. bus lines - the critical line length is even shorter.



Typical Line Impedances

The table shows typical Inductive and Capacitive Layers (L', C') of various signal traces. The last two columns display the corresponding impedance and propagation delay time along the wire calculated from L' and C'.

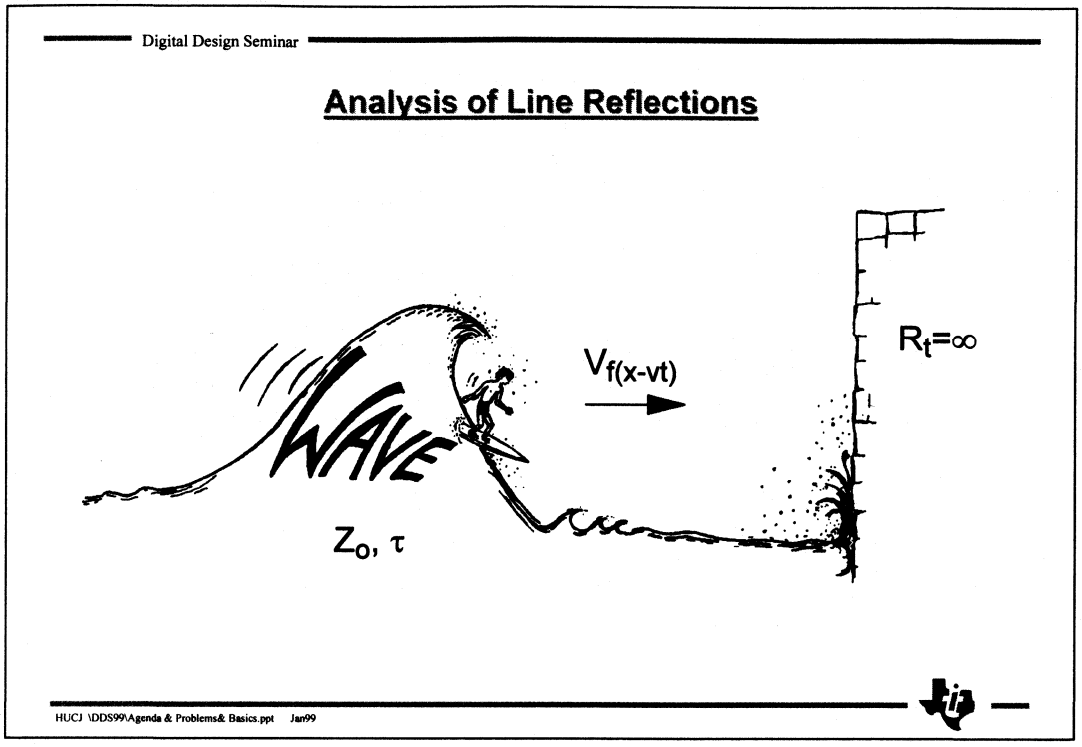
Common signal traces show an impedance in the range of 20Ω to 120Ω and propagation delay times of 4ns/m to 20ns/m.



Wave-forms with Transmission line and Capacitance Loads

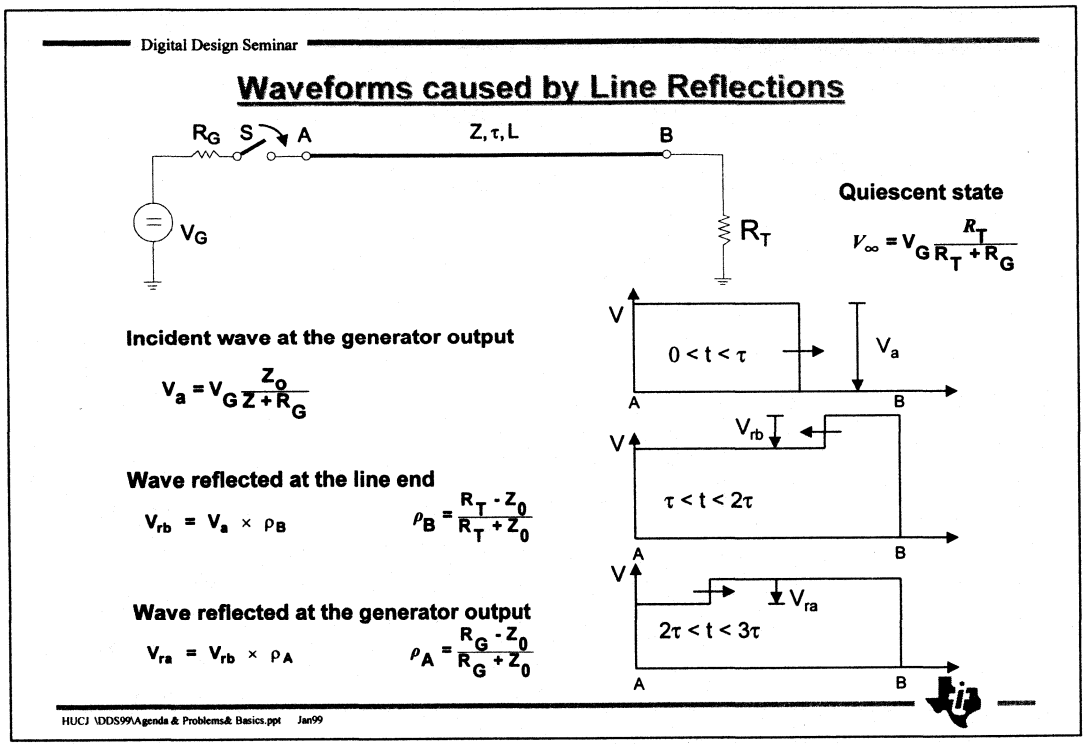
Transmission line theory says that the line impedance is independent of the line length. As a consequence, the loading of the integrated circuit connected to a transmission line must be independent of the line length. The oscillogram above shows the signal wave-forms measured at the output of an integrated circuit (SN74LS00) when terminated transmission lines of various lengths (l = 0 m, l = 1 m, l = 11 m) are connected to the output of the circuit (the line termination is required to avoid line reflections). The three signals measured are displayed with a time offset for visibility. In all cases the rise time of the signal - and that means also the propagation delay time of the integrated circuit - is not influenced by the line length, i.e.: By the capacitance of the line. However, the designer has to consider the propagation time of the signal on the transmission line: a line length l = 11 m results in signal propagation time t_p = 55 ns.

A simple capacitive load caused by a high input capacitance of the following circuit - e.g. when driving the gate of a MOS power transistor (Miller effect) - in conjunction with the output impedance of the gate (R_0 ≈ 150 Ω for a SN74LS00) generates a low-pass filter, which increases the propagation delay time of the circuit.



Analysis of Line Reflections

In data transmission systems the designer has to take care of line reflections caused by improperly terminated lines. These line reflections may lead to an additional signal distortion which would cause incorrect detection of the value of the signal at the line end (receiver input). This may result in an false operation of the system.



Wave-Forms Caused by Line Reflections

The circuit above shows a simple arrangement to analyse the wave-form in transmission circuits. At the time the switch at the output of the voltage source (generator) is closed, the effective generator load is the impedance of the transmission line alone. The voltage of the incident wave $Va_{(t=0)}$ can be calculated by using the simple voltage divider formula:

$$V_{a(t=0)} = V_o \frac{Z_o}{Z_o + R_o}$$

When the wave with this amplitude arrives at the line end, the energy not absorbed in the termination resistor - assuming that the line is not terminated correctly ($R_t \neq Z_O$) - will be reflected back to the generator. The amplitude of the reflected wave at that point is calculated:

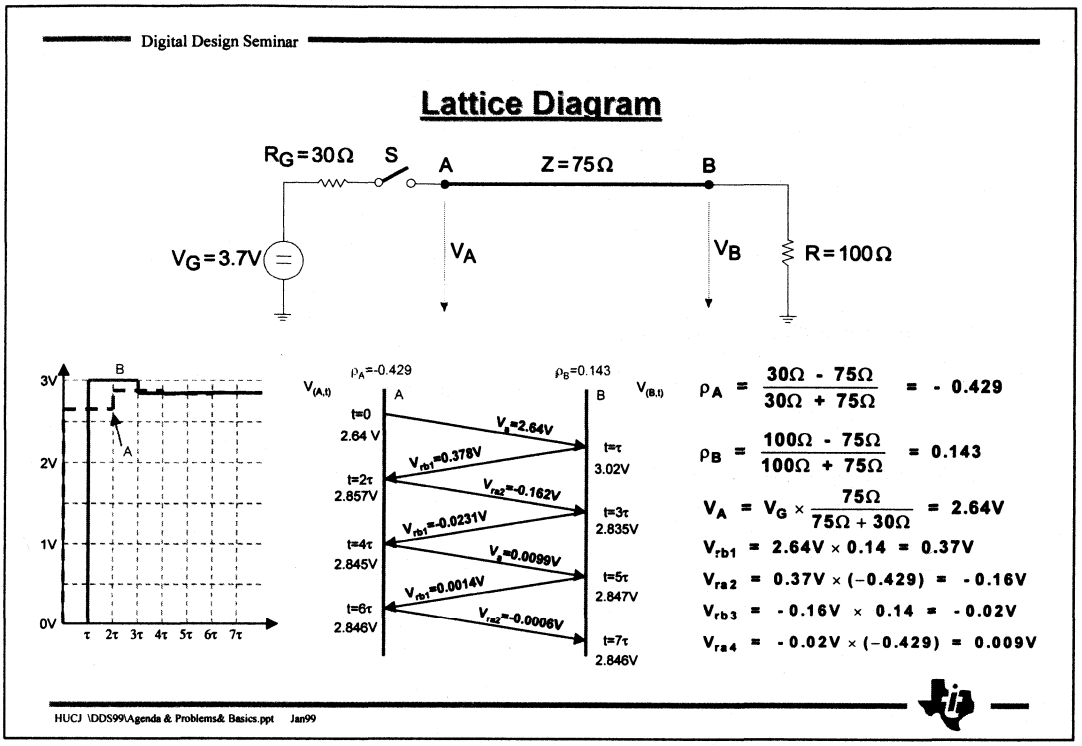
$$V_{r1} = V_a \cdot \rho_B = V_a \frac{R_t - Z_o}{R_t + Z_o}$$

When this reflected wave arrives again at the generator output and the output impedance of the generator is not equal to the line impedance ($R_O \neq Z_O$), again a reflection occurs, where the amplitude of the reflected wave has to be calculated:

$$V_{r2} = V_{r1} \cdot \rho A = V_a \frac{R_o - Z_o}{R_o + Z_o}$$

This process is continued until the energy of the wave is absorbed by the losses of the circuit (termination resistor R_t at the line end, and output resistor of the generator R_O). The final steady-state condition is calculated by the simple voltage divider:

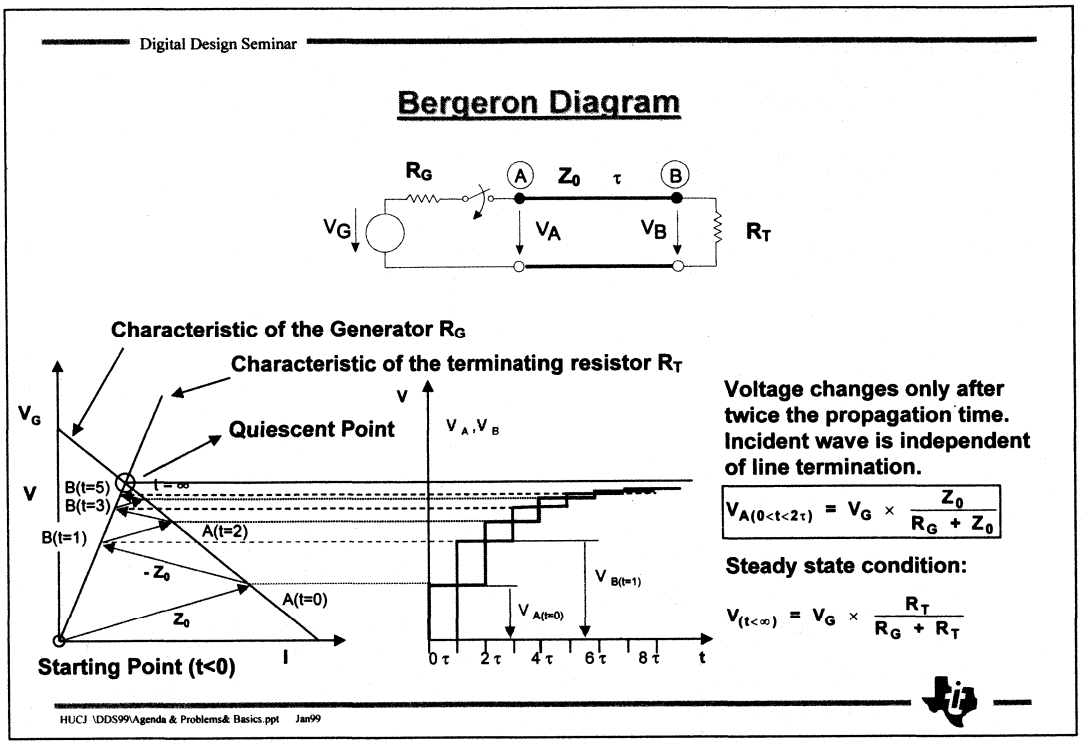
$$V_{t=\infty} = V_o \frac{R_t}{R_o + R_t}$$



Lattice Diagram

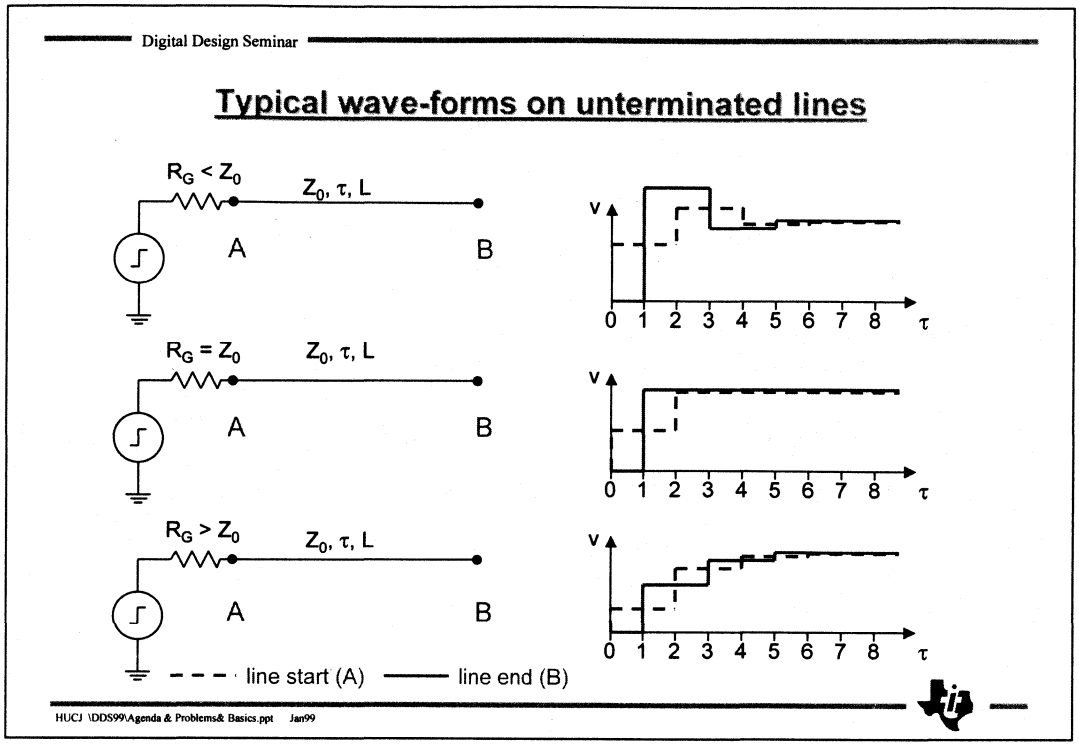
This example shows the analysis of an actual circuit. The generator with an open loop voltage V_O = 3.7 V and an output impedance R_O = 30 Ω represents the simplified equivalent circuit of a SN74F00 in the high state. The line with an impedance Z_O = 75 Ω may be a coax cable or a printed wire on multi-layer printed circuit board. As one can see, the amplitude of the reflected wave drops very fast. In most application the calculation of the various reflected waves can be stopped after the third reflection since the amplitude of the reflected wave is now so small that it can be neglected (in this example V_{rb3} = 0.02 V).

The Lattice Diagram is a useful tool to simplify handling the many numbers to be considered when analysing line reflections. In this simple example the diagram consists of two time scales, each representing the situation at the beginning and at the end of the line. A change of voltage at the generator output is found at every even multiple of the propagation time, at the end of the line at every odd multiple of the propagation time. These points are now connected by lines which represent the forward and backward travelling waves. To each of these lines the corresponding voltage is assigned. The final task left is to add these voltages at the left side of the diagram (beginning of line) of the right side (end of line) to calculate the voltage in the system at a specific time.



Bergeron Diagram

The Bergeron Diagram is a simple tool to analyse line reflections in circuits which show non-linear characteristics e.g. semiconductor components. For the analysis one has to draw a voltage/current diagram. Into this diagram the output characteristic of the generator R_0 (in this example a linear resistor) as well as the characteristic of the termination at the line end R_t has to be drawn. The point of intersection of these two lines provides the first result: the steady state voltage. The steady-state condition on the line before the switch has been closed ($V_{t=0}$ = 0 V, $I_{t=0}$ = 0 mA) is the starting point for the construction of the wave-form. Through this point (in this example the origin of the diagram) a line with the slope of the line impedance Z_0 (tg $\alpha = Z_0$) is drawn. Where this line hits the line which represents the output characteristic of the generator A(0), one gets the voltage of the incident wave. By drawing a line with the negative slope (tg a = $-Z_0$) through the point just constructed, the point of intersection (B_{tp}) with the line representing the termination characteristic R_t provides the voltage at the line end, when the wave arrives there the first time. By further drawing lines with alternating slopes (Z_0, $-Z_0$) one finds the voltages in the circuit during the following build-up. Finally the wave-forms at the beginning and the end of the line can be constructed by using the voltages found during the previous construction.



Typical wave-forms on unterminated lines

$R_G < Z$:

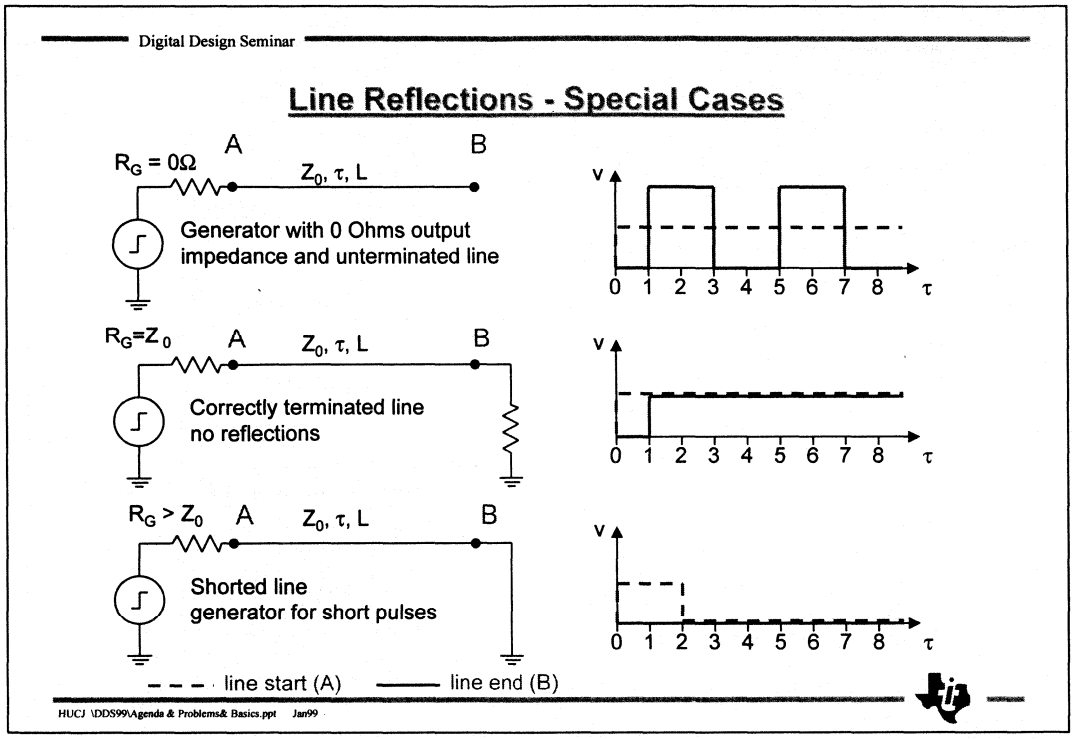
The resistor devider R_G and Z determined the amplitude of incident wave. In this case the amplitude is higher that 50% of the full voltage swing. This signal is 100% reflected at the unterminated end of the line, this means that it is doubled. Thus a overshoot can be seen at the line end. A negative reflection factor at the line-start generated a undershoot when the reflected wave arrives.

$R_G = Z$:

Two equal resistors generate a incident wave with exactly half of the full voltage swing. Again the incident wave is 100% reflected at the line-end, hence the voltage doubles. The amplitude of the incident and the reflected wave together result in exactly the full generator voltage swing.

$R_G > Z$:

The high output impedance of the generator limits the amplitude of the incident wave to less that 50% of the generator amplitude. Thus the sum of the incident wave and the reflected wave are less than 100%. It takes several signal delay times to reach the final high level.

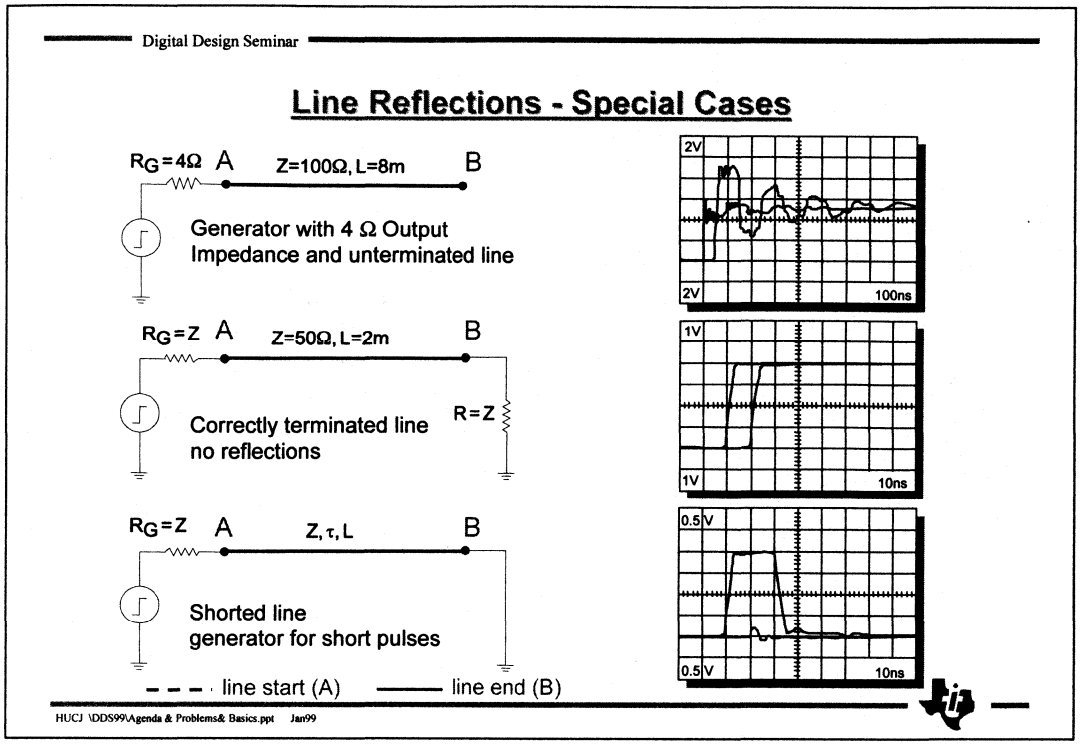


Line Reflections - Special Cases

This picture shows various extreme situations in transmission circuits. In the first circuit a generator with zero ohm output impedance (R_O = 0Ω) drives a loss-free transmission line, with an open circuit at the line end ($R_t = \infty$). The open circuit may represent the input impedance of integrated circuits, which mostly have an input impedance of several kilo-ohms - large compared with typical line impedance. The reflection factor ρ = -1 at the generator output and ρ = 1 at the line end leads to an undamped oscillation at the end of the line. This causes a receiver to switch many times, not once only as desired.

The next circuit shows an interface terminated correctly at the line end. Under this condition one finds an undistorted signal (no line reflections)

The last circuit shows an interface shorted at the line end. For simpler understanding the output impedance of the generator has been chosen to be equal to the line impedance ($R_O = Z_O$). When the switch is closed, an incident wave with an amplitude of $0.5 \times V_O$ travels to the line end and is reflected there with the inverted amplitude (ρ = -1). When the reflected wave arrives at the generator output again the steady-state is achieved. This circuit is a pulse generator which provides a pulse width equal to twice the propagation time of the wave on the transmission line. Such a circuit can be used advantageously when pulses with a length of a few nanoseconds only have to be generated.

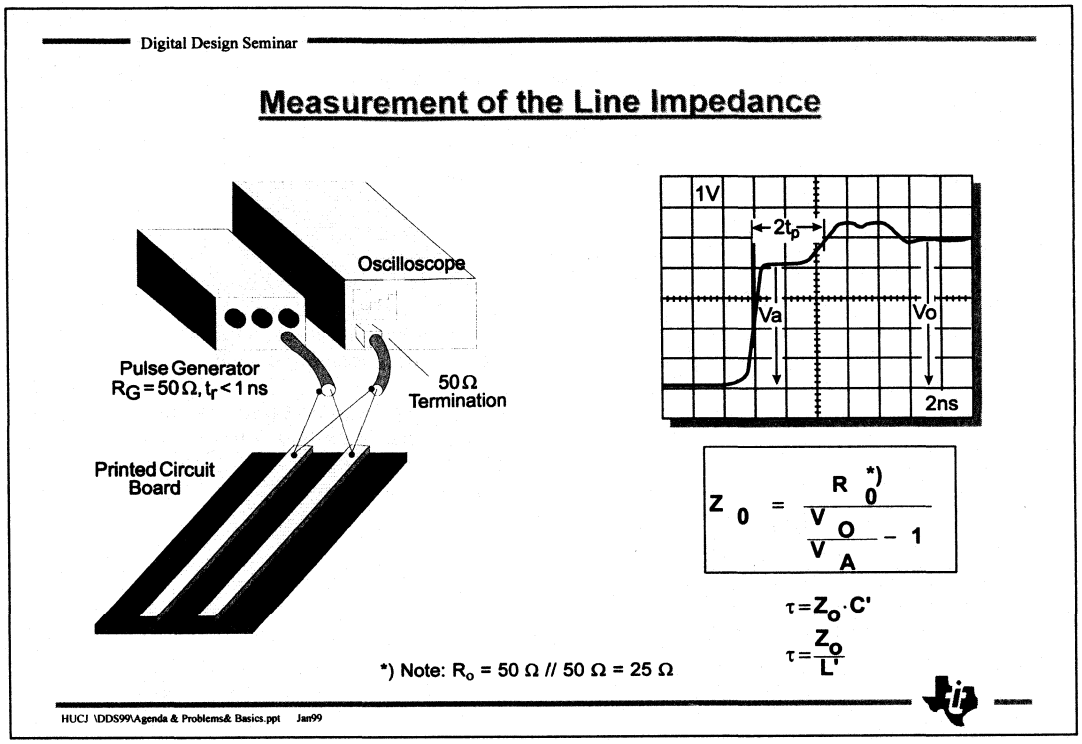


Line Reflections - Special Cases

The circuits described before have been built up to vary the behaviour. It is not as easy to design an generator with an output impedance of 0Ω. Therefore an Advanced CMOS circuit has been used as the generator. Its output impedance R_O = 8 Ω leads to a damped oscillation, where the first undershoot at the line may still be capable of reaching the threshold voltage of the receiver to cause a false triggering.

The correctly terminated line shows no signal distortion.

In the interface shorted at the end, a coax cable with a propagation time t_p = 5 ns/m and a length l = 2 m has been used. This circuit generates a pulse with a width t_d = 2 × 5 ns/m × 2 m = 20 ns.



Measurement of the Line Impedance

For correct design of an interface (selection of the generator, termination of the transmission line), knowledge of the impedance of the transmission line in use is necessary. One way to determine the line impedance is by means of a L/C bridge where one measures the inductance of a transmission line shorted at the end (short circuit impedance ≈ inductive layer L') and capacitance with the line open at the end (open circuit impedance ≈ capacitive layer C'). This method however mostly requires expensive equipment which often is not available.

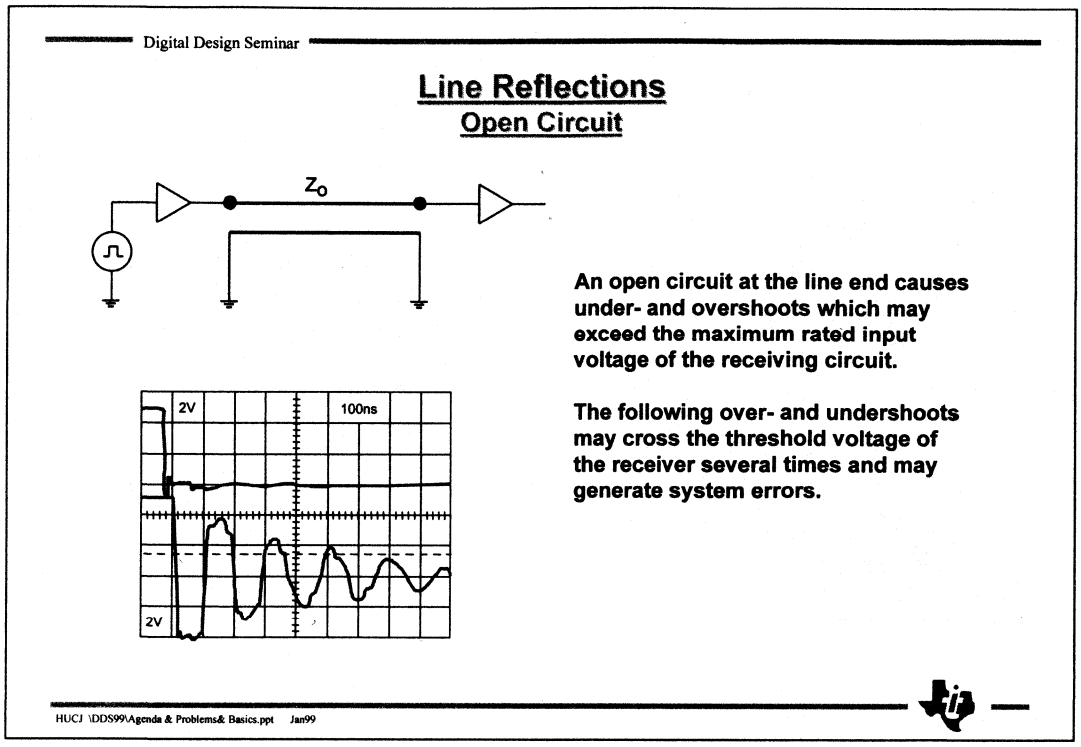
A simpler method is shown on the picture above, where one needs a fast pulse generator and an oscilloscope only. By applying this method one measures the amplitude of the incident wave V_a caused by the voltage divider 'output impedance of the generator / line impedance' (in this example a signal and a ground wire in parallel on a printed circuit board) as well as the steady-state voltage V_O. By using the following equation (the voltage divider formula solved to Z_O) one gets the line impedance Z_O:

$$Z_o = \frac{R_o}{\frac{V_o}{V_a} - 1}$$

where R_O is output impedance of the generator. In this measurement set-up the output impedance is made by the two coax cables in parallel, therefore R_O = 25 Ω.

By measuring the propagation time t_p one can also determine the inductance and the capacitance per unit length:

$$L' = t_p \cdot Z_o \qquad C' = \frac{t_p}{Z_o}$$



Line Reflections - Open Circuit

Driving an unterminated transmission line with a low-impedance output generates a good signal quality at the beginning of the line, while at the end of the line oscillation can be observed. This corresponds to the first example of our “Special Cases”.

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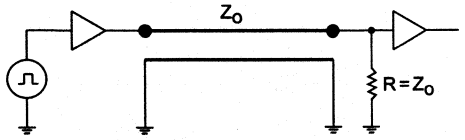
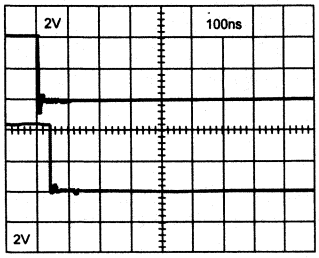
Line Reflections
Terminated Line





Line reflections are eliminated by correct line termination.

A mismatch up to 50% is acceptable.

Note: - Increased Power Dissipation
- High drive Capability required.

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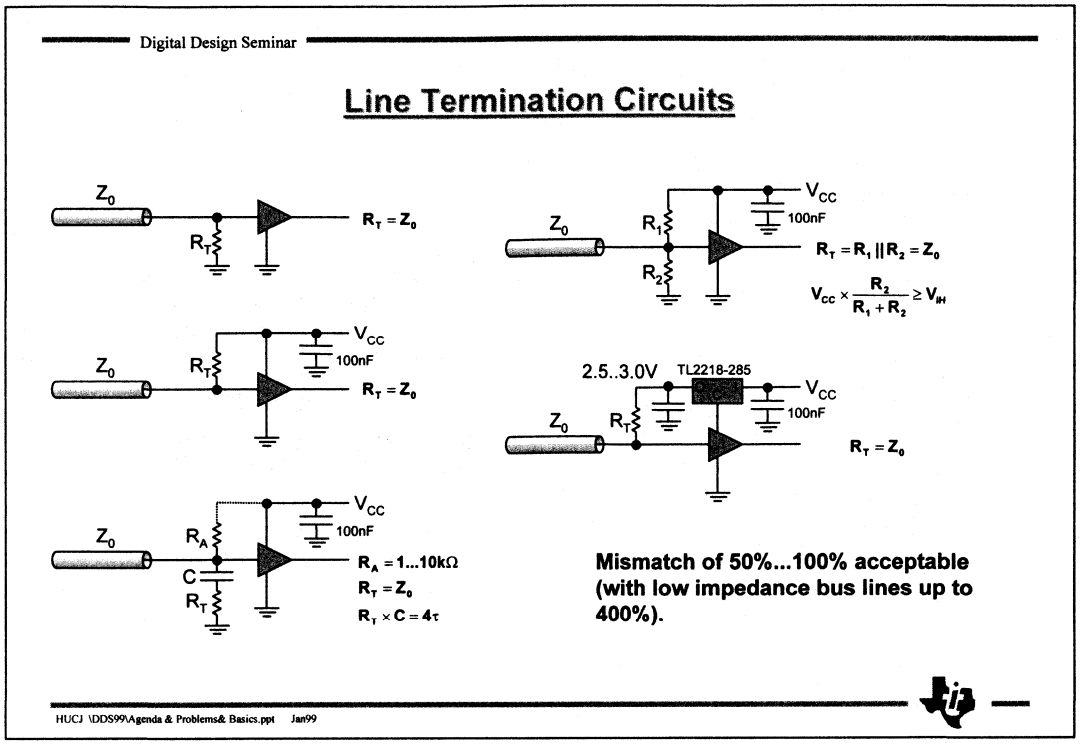
Line Reflections - Parallel-Terminated Line

Transmission lines are parallel-terminated at the line end by a resistor between the signal line and the signal return line. If the termination resistor is chosen equal to the line impedance ($R_t = Z_O$) no line reflections are found. In many applications, a mismatch of up to 50 % is acceptable. Under this condition the resulting reflection factor will be $\rho = 0.2$.



Parallel Line Termination Circuits

Single-ended or unbalanced transmission lines are usually terminated by a resistor between the line end and signal ground. If the drive capability of the generator in high state is not sufficient - e.g. open collector or open drain outputs - the termination resistor can also be placed between the line and the positive supply rail. This rail for low frequencies is shorted to ground via the power supply and for high frequencies via the decoupling capacitor (typical 0.1 µF).

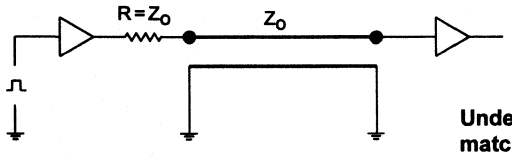
Particularly in CMOS applications, the designer does not like the continuous current in the termination resistor. This current increases the power dissipation. The current can be blocked by placing a capacitor C_b in series with the termination resistor R_t. When the time constant $R_t \times C_b$ is about 4 times the propagation time of the interface circuit, the line is almost sufficiently terminated.

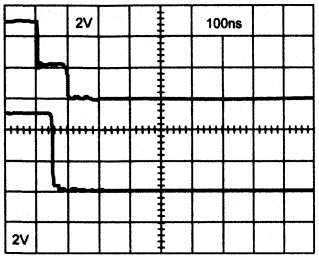
In TTL systems, a resistor divider is often found at the line end (split resistor or Thevenin termination). This circuit is adapted ideally to the drive capability of TTL circuit and performs well in terms of eliminating line reflections. However the disadvantage of this arrangement is the large DC current through the resistor divider.

In advanced interfaces therefore a circuit is often used, which is called active termination. Here the termination resistor is placed between the line end and the output of an additional power supply, which provides an output voltage of 2.5 - 3 V. Since on average 50 % of its active time the line is in the high state, the supply current is reduced by this amount. This termination technique is also used in bus applications, where much of the operating time all bus drivers are in inactive mode (3-state). In this situation the supply current becomes zero. Last but not least, the pull-up resistor avoids the line floating when all bus drivers are in the 3-state.

Line Reflections

Matching of Generator Impedance with Serial Termination





Under- and overshoots are avoided by matching the output impedance of the line driver to the line impedance by means of a series resistor. Power dissipation is not increased (recommended in CMOS systems).

Note: Undefined logic levels along the transmission line for up to twice the propagation time.

Circuits with built-in serial termination (25Ω to 30Ω):
8 Bit: SN74ABT2244
16 Bit: SN74ABT162244
18 Bit: SN74ABT162501

Line Reflections - Matching of Generator Impedance

An elegant method to avoid under and overshoots at the line end is to match the output impedance of the driver circuit to the line impedance by placing a resistor in series with the output. A different output impedance of the driver in the low and the high state mostly does not allow correct matching. As long as the output impedance of the circuit in question is chosen to be 60 % to 100 % of the line impedance, a reasonable signal quality can be expected at the line end (receiver input). This technique is applicable in uni- and bi-directional point-to-point interfaces. In multi-point applications, where several stations are located along the transmission line, this technique is not recommended due to the long settling time of the signal (up to twice the propagation time).

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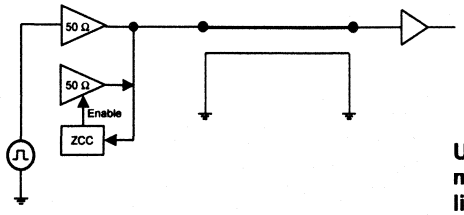
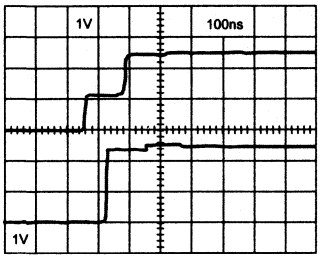
Line Reflections

Matching of Generator Impedance with DOC™ Circuit





Under- and overshoots are reduced by matching the output impedance of the line driver to the line impedance during transition by means of a temporarily switched parallel driver.

Note: Undefined logic levels along the transmission line for up to twice the propagation time.

All members of the SN74AVCxxx family include the DOC™ circuit in the output stages

DOC is trademark of Texas Instruments Incorporated

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The DOC™ Circuit consists of the combination of two 50 Ohm output stages : One output stage works constantly, while the second one is only temporarily switched in parallel during the transition phase. This means that in the static 'LOW' and 'HIGH' cases only one output stage is active. The other parallel-switched 50 Ohm output stage is controlled by the Impedance Control Circuit (ZCC), which only activates the second output stage during the transitions from 'LOW' to 'HIGH' and from 'HIGH' to 'LOW'.

The behavior is split into 3 phases:

Phase 1 (High Impedance) :

The output of the device is in the 'LOW' state. One 50 Ohm Output stage is active only. The second stage, which is controlled by ZCC, is in high impedance. The output impedance is in the range of 50 Ohms.

Phase 2 (Low Impedance):

The ZCC watches the output. During the transition phase it switches the second 50 Ohm driver in parallel. The characteristic impedance of the parallel circuit of both 50 Ohm drivers is equivalent to a 25 Ohm output stage. This resulting in a high output current which therefore enables a very fast switching signal.

Phase 3 (High Impedance) :

Apon reaching the threshold value (in high direction) the ZCC controlled 50 Ohm driver is switched to a high impedance state. The output impedance of the device is increased back to about 50 Ohms.

For the switching into the opposite direction the circuit behaves in an analog way.

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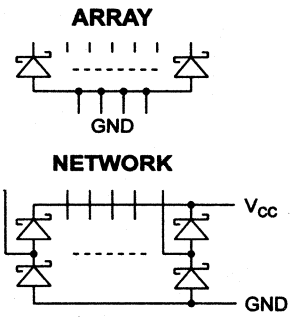
Bus Termination Arrays

Released Functions :
SN74S1050 12-Bit Schottky Diode Array
SN74S1051 12-Bit Schottky Diode Network
SN74S1052 16-Bit Schottky Diode Array
SN74S1053 16-Bit Schottky Diode Network
SN74S1056 8-Bit Schottky Diode Array
SN74F1056 9-Bit Schottky Diode Array
SN74F1016 16-Bit Schottky Diode R-C Bus Termination Array
SN74F1018 18-Bit Schottky Diode R-C Bus Termination Array



Applications :
- ★Arrays in TTL systems
- ★Networks in CMOS systems (positive overshoots)
- ★Small buses, e.g. Memory Arrays
- ★System bus in personal computers

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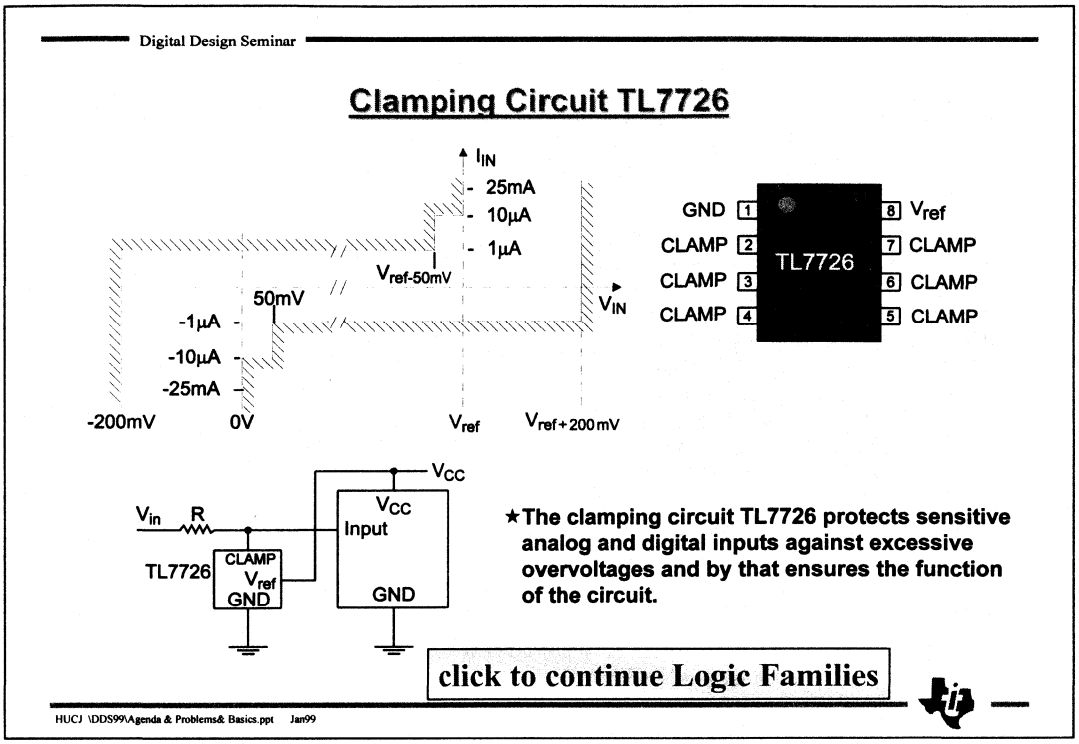
Line Reflections - Bus Termination Arrays

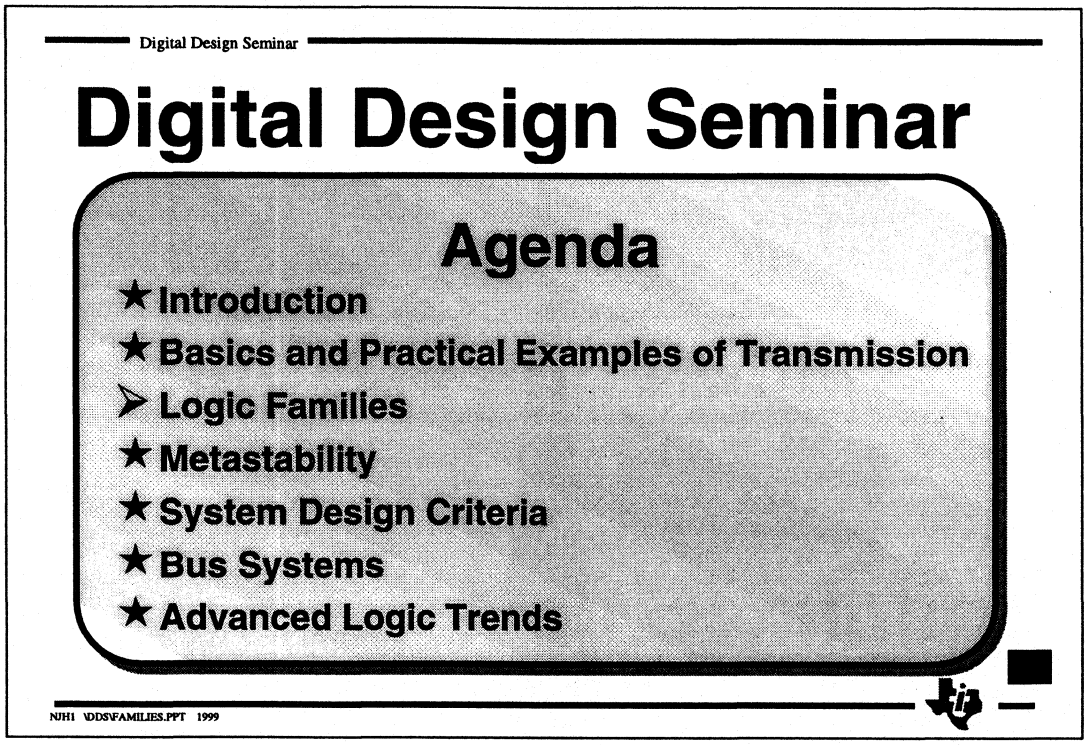
To reduce the number of required components, Texas Instruments offers the Bus Termination Arrays:

These circuits include clamping diodes for 8- to 16-Bit circuits. Depending on the device type, the designer can select between clamping diodes to GND only or two rows of clamping diodes, one to V_{CC} and one to GND.



Line Reflections - Clamping Circuit TL 7726

The clamping circuit TL7726 protects sensitive analog and digital inputs against excessive overvoltages and thus ensures the function of the circuit. It limits the over- and under-shoots to a maximum of +/-200mV by sourcing up to 25mA of clamping current.


Digital Design Seminar
Digital Design Seminar
Agenda
★ Introduction
★ Basics and Practical Examples of Transmission
➢ Logic Families
★ Metastability
★ System Design Criteria
★ Bus Systems
★ Advanced Logic Trends
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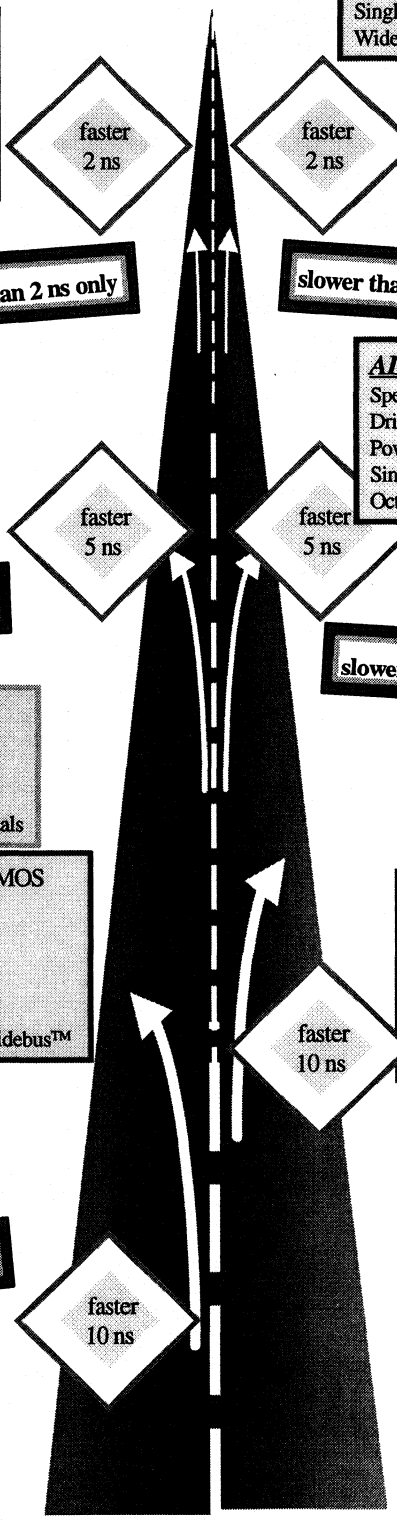
5-V TI Logic Road 3.3-V



CBTLV CMOS
Speed: max 250 ps
Drive : no drive
Power: 20uA
Single Gate, Octals and Widebus™

AVC CMOS
Speed: max 1.7 ns
Drive : ±12mA (Static + DOC™
Power: 40uA
Single Gates, Gates, Octals, Widebus™ , LFBGA

CBT CMOS
Speed: max 250 ps
Drive : no drive
Power: 50uA
Single Gate, Octals and Widebus™

ALB BiCMOS
Speed: max 2.0 ns
Drive : ± 25 mA
Power: 800uA/5mA (per Buffer)
Widebus™

ALVT BiCMOS
Speed:max 2.4 ns
Drive : -32/64mA
Power: 100u /5mA
Widebus™
5V tolerant

ALVC CMOS
Speed: max 3.0 ns
Drive : ± 24mA
Power: 40uA
Single Gate, Gates, Octals, Widebus™, LFBGA

ABT BiCMOS
Speed: max 3.9 ns (Octals)
max 3.5 ns (Widebus)
Drive : -32/64 mA
Power: 250uA/30mA
Octals , Widebus™, Widebus + ™

LVT BiCMOS
Speed:max 4.0 ns
Drive : -32/64mA
Power: 190u /5mA
Octals and Widebus™
LFBGA
5V tolerant

AS Bipolar
Speed : max 6.2 ns
Drive : -15/64 mA
Power: 59 mA
Gates, Flip-Flops, Octals

74 F Bipolar
Speed :max 6.2 ns
Drive : -15/ 64mA
Power: 80 mA
Gates, Flip-Flops, Octals

LVC CMOS
Speed: max 6.5 ns
Drive : ± 24mA
Power: 10uA
Single Gate, Gates, Flip-flops
Octals, Widebus™, LFBGA
5V tolerant

ACT CMOS
Speed: max 7ns
typ. 3.5 ns
Drive : ± 24mA
Power: 40uA
Gates, Flip-Flops,
Octals and Widebus™
Endpin and Centerpin

AHCT CMOS
Speed : max 8.5
typ. 5.4 ns
Drive : ± 8mA
Power: 40uA
Single Gates, Gates,
Flip-Flops,Octals, Widebus™

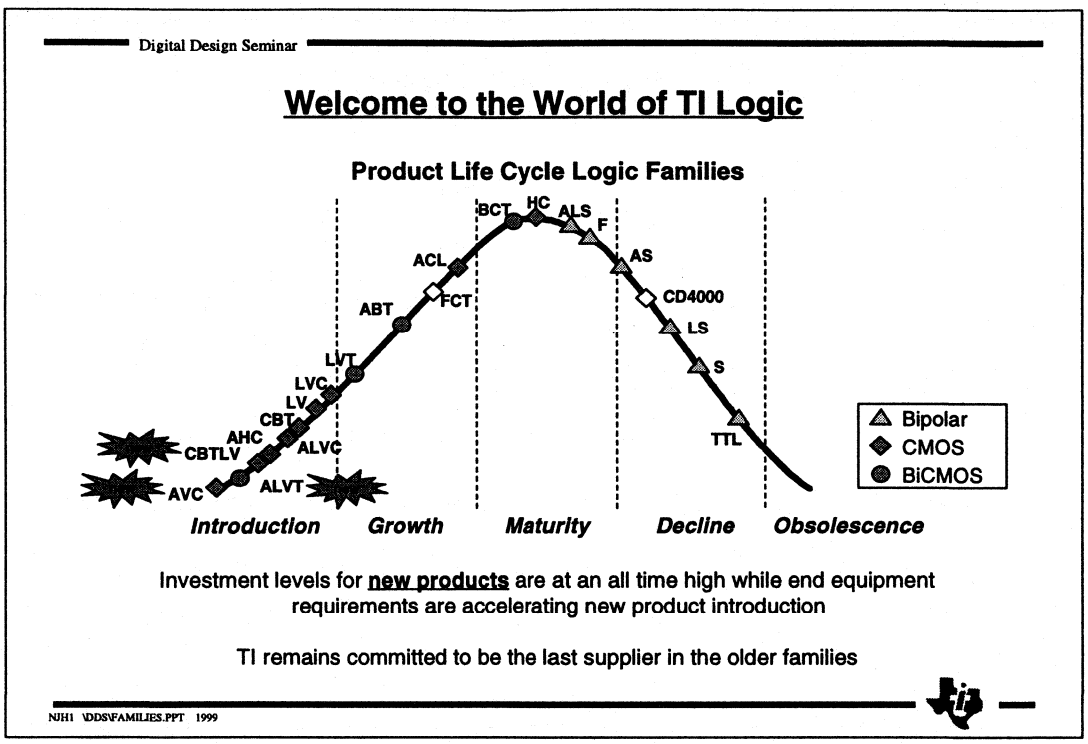
AC CMOS
Speed: max 9 ns
Drive : ± 12mA
Power: 40uA
Gates, Flip-flops
Octals and Widebus™
(designed for 5V)

AHC CMOS
Speed : max 9.5ns
Drive : ± 4mA
Power: 40uA
Single Gate, Gates,
Flip-Flops,
Octals and Widebus ™
5V input tolerant

ALS Bipolar
Speed : max 10ns
Drive : -15/64 mA
Power: 50 mA
Gates,Flip-Flops,Octals

LV CMOS
Speed: max 10 ns
Drive : ± 8mA
Power: 20uA
Gates, Flip-Flops,
Octals
5 V Tolerant

HCT CMOS
Speed: max 20 ns
Drive : ± 8mA
Power: 80uA
Gates,Flip-Flops,Octals



The Product Life Cycle curve shows all the available logic families from TI.

This cycle is divided into 5 sections, beginning on the left side with the introduction phase and ending on the right side with obsolescence.

One finds that all bipolar families are in the decline phase. These are not recommended to be used in new designs.

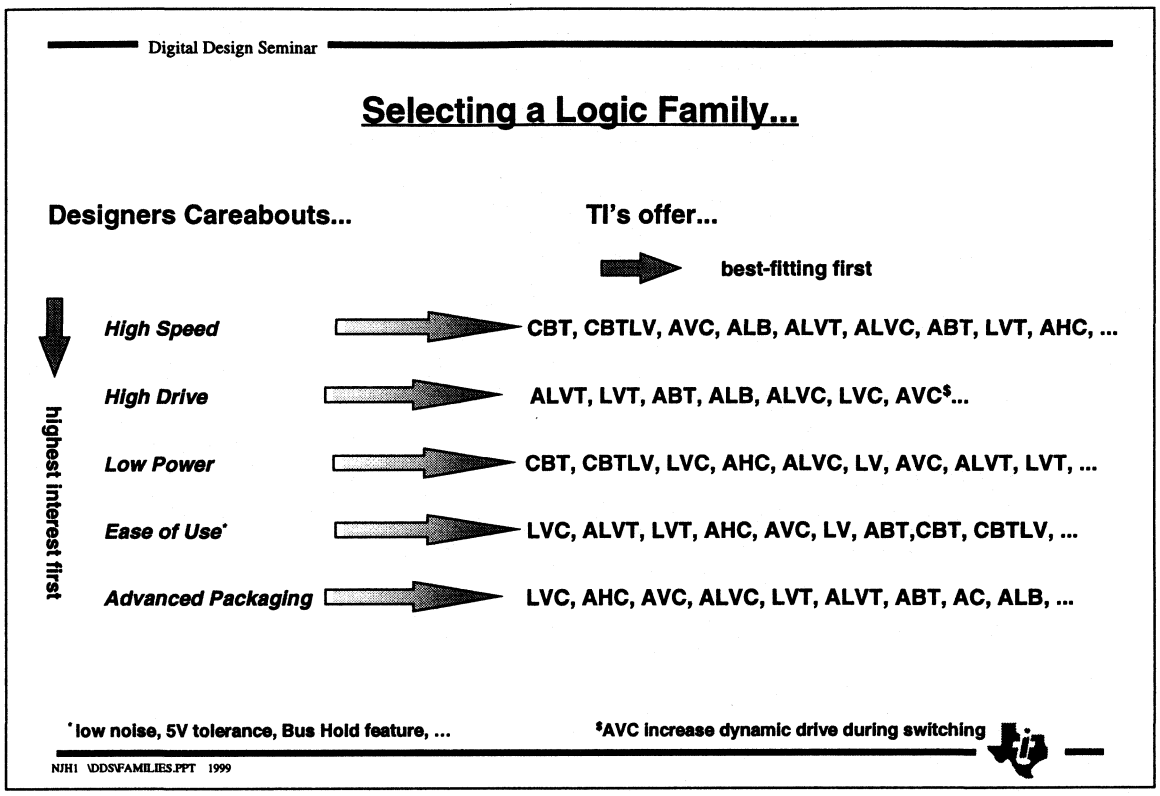
Today's system trends, such as increased packaging density, higher operating frequencies and reduced heat generation (e.g. no need for a cooling fan), lead to a strong need to reduce the power consumption or to change to low power technologies. This limits the use of mature technologies like LS and F. Even for HCMOS there is an improved version available: AHC Advanced HCMOS.

With the development of BiCMOS, a combination of Bipolar and CMOS technologies, the high drive capability and low noise characteristic of bipolar technology and the low power consumption of CMOS technology have been combined.

TI has true second source agreements with Philips Semiconductor and Hitachi Semiconductor for the Advanced BiCMOS Technology (ABT) family as well as for the low-voltage families (LV, LVC, LVT, ALVC). The agreement with Philips has recently been extended to also cover ALVT, AHC and the newest member to the TI portfolio AVC Advanced Very-Low-Voltage CMOS family.

Investments for new products are at an all time high while end equipment requirements are accelerating new product introduction.

On the other hand, TI remains committed to be the last supplier in the older families.



Customer careabouts for selecting the optimum logic family are diverse depending on application needs and targeted end-equipments. From a survey recently conducted by TI, the ranking of customer careabouts are as shown above.

According to this survey, the careabouts have been sorted by importance from top to bottom.

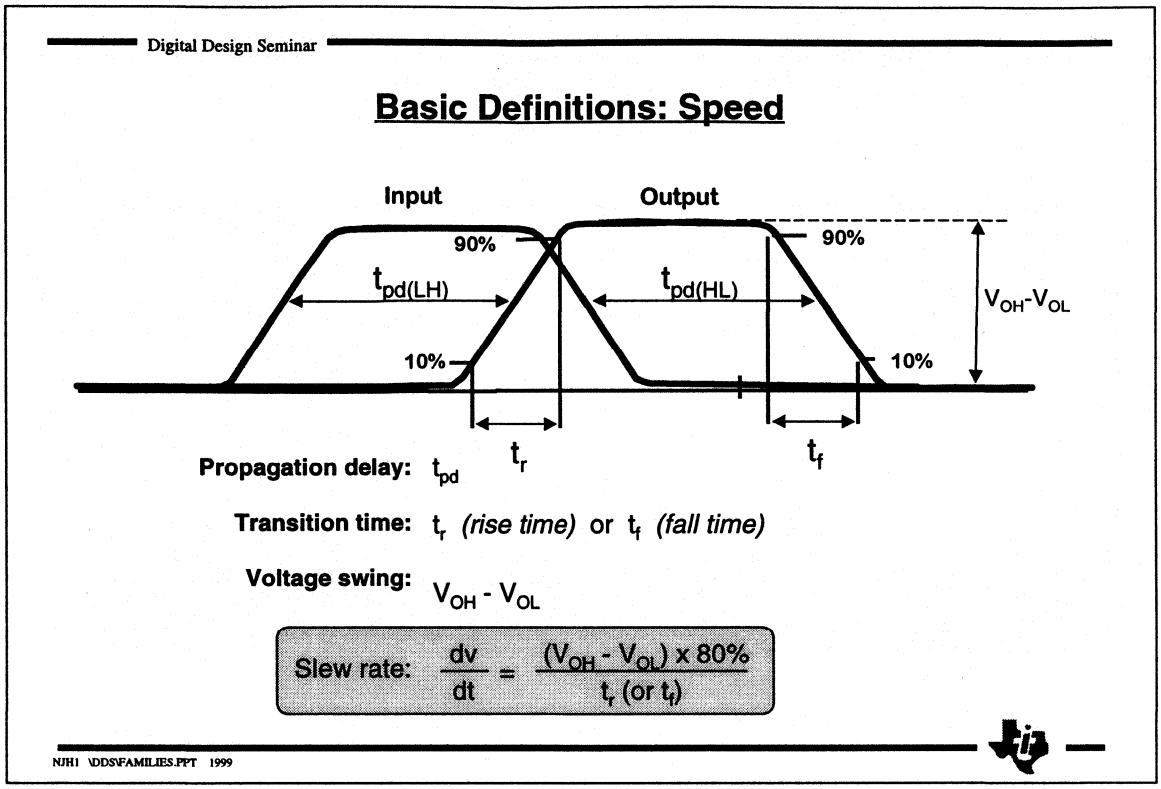
The logic families have been sorted from left to right with regard to the most suitable family for a given criterion.

For example: Are you looking for the fastest logic family ?

Choose the row 'High Speed' and look for the first family in 'TI's offer': ALB

(CBT and CBTLV have no output drive capability).

It doesn't matter which focus you have; TI offers always the optimum logic family for your application.



There are two parameters a designer may have in mind when mentioning "speed". The most frequently used refers to the circuit's propagation delay, tpd.

- **The shorter the t_{pd}, the higher the speed.**

Some engineers, however, also refer to "circuit speed" in the context of a device's signal slew rate. As can be seen from the formula, a circuit's slew rate corresponds to the transition (rise or fall) time of the output signal.

- **The shorter the rise or fall time, the higher the slew rate.**

As will be shown on the next page, propagation delay and slew rate are not necessarily proportional.

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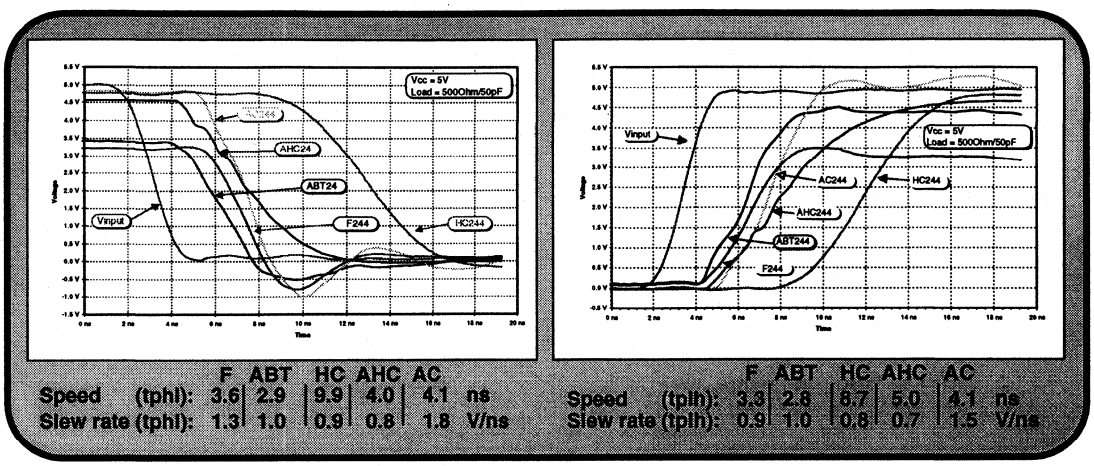
Switching Characteristic
Slew Rate - 5-V Logic



	F	ABT	HC	AHC	AC	
Speed (tphl):	3.6	2.9	9.9	4.0	4.1	ns
Slew rate (tphl):	1.3	1.0	0.9	0.8	1.8	V/ns

	F	ABT	HC	AHC	AC	
Speed (tplh):	3.3	2.8	8.7	5.0	4.1	ns
Slew rate (tplh):	0.9	1.0	0.8	0.7	1.5	V/ns

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This and the next page show propagation delays (tpd), voltage swing (V_{OH} - V_{OL}) and slew rates (dv/dt) for selected 5V and 3V logic families.

F, ABT, HC, AHC and AC operate from a 5V supply voltage, while ALVT, LVT, AVC, ALVC, LVC, AHC and LV have a 3.3V supply (next page).

The data may indicate that tpd and dv/dt show common trends, but a closer look points out that there is no direct link between the two parameters. For example, the fastest family (ABT) is not the one with the highest slew rate. Another example is **AHC, which is characterised by a three-fold speed improvement over HCMOS**, but shows lower slew rates.

As will be discussed later in this section, **high slew rates are often unfavourable**, as this leads to high noise levels generated by the components. The worst technology in this respect is 5V AC, while AHC gives very good results.

Slew rates must be considered especially when designing high speed systems.

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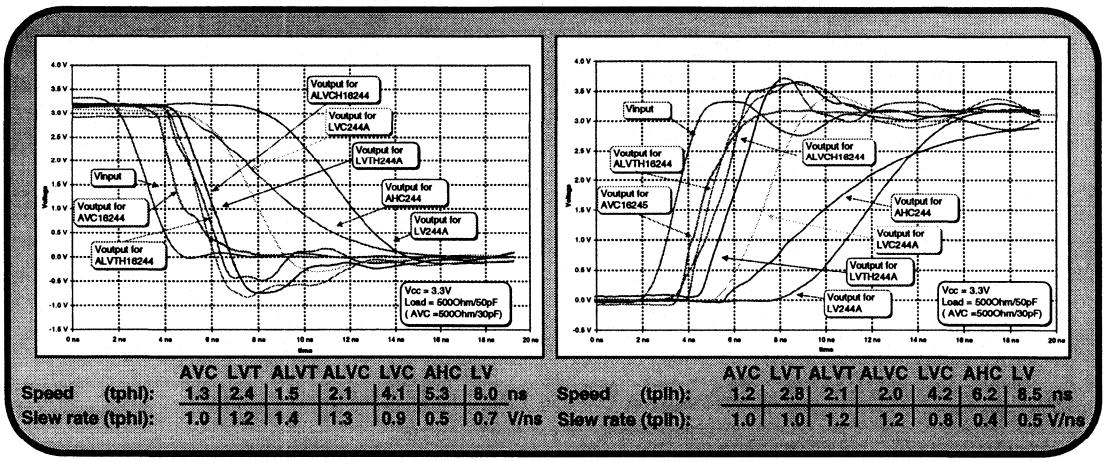
Switching Characteristic

Slew Rate - 3-V Logic



	AVC	LVT	ALVT	ALVC	LVC	AHC	LV
Speed (tphl):	1.3	2.4	1.5	2.1	4.1	5.3	8.0 ns
Slew rate (tphl):	1.0	1.2	1.4	1.3	0.9	0.5	0.7 V/ns

	AVC	LVT	ALVT	ALVC	LVC	AHC	LV
Speed (tplh):	1.2	2.8	2.1	2.0	4.2	6.2	8.5 ns
Slew rate (tplh):	1.0	1.0	1.2	1.2	0.8	0.4	0.5 V/ns

AVC contains TI's revolutionary Dynamic Output Control (DOC) circuitry that automatically lowers the output impedance of the circuit during a signal transition and subsequently raises the impedance after signal transmission to reduce noise.

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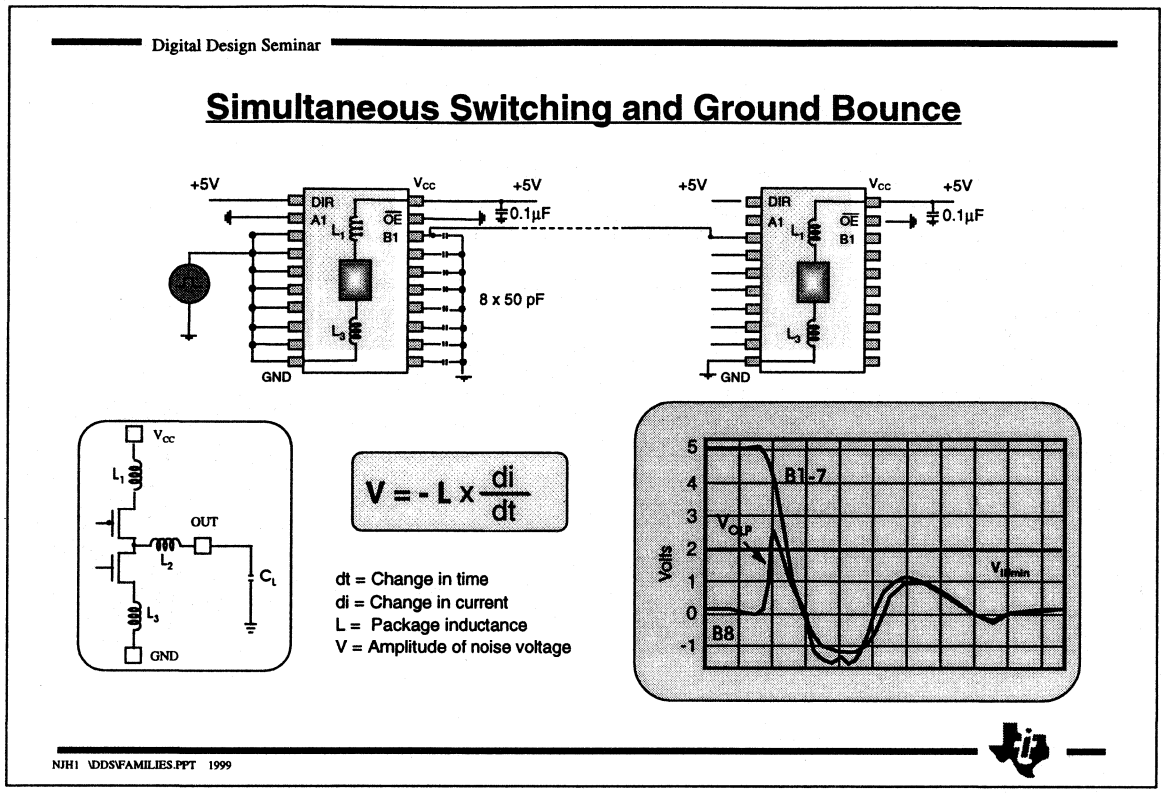
These graphs show propagation delays (tpd), voltage swing (V_{OH} - V_{OL}) and slew rates (dv/dt) for selected 3V logic families (AVC, LVT, ALVT, ALVC, LVC and LV) and AHC operated at V_{CC}=3.3V (as specified in the datasheet).

In comparison with 5V logic, **all the low voltage technologies have somewhat lower signal slew rates.**

It should be especially noted that **AVC**, the fastest of all technologies shown, exhibits one of the lowest slew rate of all the low-voltage logic families.

Circuit design techniques and the use of SSOP or TSSOP packages enable the user to benefit from this favourable characteristic.



A widely accepted method of measuring ground bounce is to switch N-1 device outputs, while keeping the Nth input at a LOW level.

The outputs of the drivers which are switching, react after a certain delay to the changes at the inputs, whilst **the unswitched output should remain undisturbed at the LOW level**. But crosstalk from the neighbouring pins, a brief dip in the supply voltage and a brief rise of the ground level (resulting from the inductance of the V_{CC} and ground connections) automatically cause a reaction at the corresponding output.

The **lowest ground bounce is achieved by the 48 pin Widebus™ package**. This is primarily because of the 8 distributed GND pins for the 16 integrated drivers. The traditional 8 bit 'corner pin' devices are provided with only one GND pin and therefore show poorer behaviour.

It is also necessary to mention that the measured values of noise level depend on the process technology used.

Whereas with BiCMOS and bipolar devices the threshold level will normally not be exceeded, with fast CMOS logic 2V or more may be reached as a result of the steeper pulse slope of the CMOS signals, with a consequently higher effect of the lead inductance.

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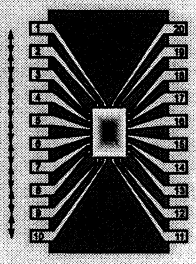
Package Inductance drives Noise Voltage

- ★ Noise levels depend on package inductance and current slew rates (di/dt)
- ★ Noise voltages induced in switching outputs will be cross-coupled into quiet output(s)
- ★ Packages with multiple V_{CC}/GND pins (e.g. Widebus™) typically show much lower noise
- ★ Slew rate control helps reduce noise

DIP			SOP			TSSOP		
Capacitance to GND	Pin Inductance	Coupling Factor	Capacitance to GND	Pin Inductance	Coupling Factor	Capacitance to GND	Pin Inductance	Coupling Factor
1.49 pF	13.7 nH		0.85 pF	5.8 nH		0.40 pF	3.3 nH	
		0.5			0.4			0.46
1.29 pF	11.1 nH		0.75 pF	4.6 nH		0.35 pF	2.9 nH	
		0.5			0.4			0.21
0.90 pF	8.6 nH		0.60 pF	3.8 nH		0.22 pF	1.9 nH	
		0.4			0.4			0.42
0.72 pF	6.0 nH		0.54 pF	3.3 nH		0.23 pF	1.8 nH	
		0.4			0.4			0.44
0.53 pF	3.4 nH		0.45 pF	3.0 nH		0.21 pF	1.8 nH	
		0.3			0.4			0.45
0.53 pF	3.4 nH		0.45 pF	3.0 nH		0.21 pF	1.8 nH	
		0.4			0.4			0.44
0.72 pF	6.0 nH		0.54 pF	3.3 nH		0.23 pF	1.8 nH	
		0.4			0.4			0.42
0.90 pF	8.6 nH		0.60 pF	3.8 nH		0.22 pF	1.9 nH	
		0.5			0.4			0.21
1.29 pF	11.1 nH		0.75 pF	4.6 nH		0.35 pF	2.9 nH	
		0.5			0.4			0.46
1.49 pF	13.7 nH		0.85 pF	5.8 nH		0.40 pF	3.3 nH	



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There are three factors which determine the electrical characteristics of a package:

1) the capacitance of a pin to ground
2) the inductance of a pin
3) the coupling factors of the pins to each other

In particular, the supply voltage pin should have a low inductance, and all signal lines in a good package should have as low as possible of all these three parameters.

The table above shows capacitance, inductance and coupling factor of each pair of neighbouring pins. These parameters are determined by:

- *The length of the connections to the pin within the package,*
- *The spacing between these connections.*

A DIP package has significantly longer internal connections than SOP, SSOP and TSSOP. A long connection results in a high inductance and a high coupling factor; the increased area caused by the long connections also results in a high capacitance.

However, the reduction in coupling factor achieved by the short connections is partly offset by the smaller spacing between them.

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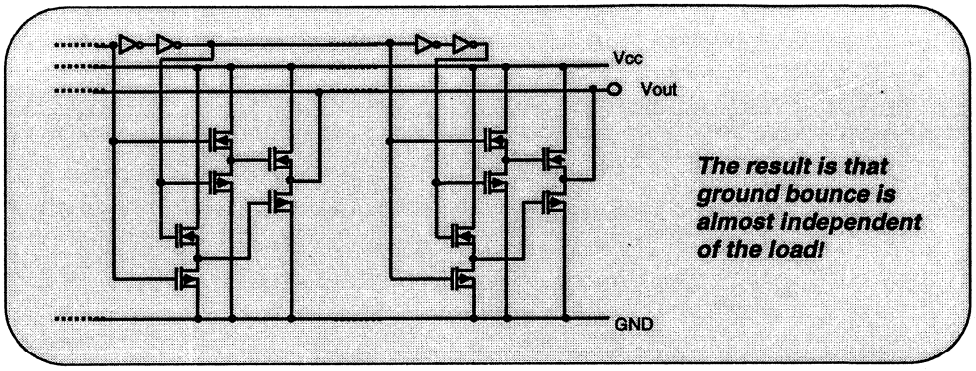
Output Edge Control Circuitry (OEC™)

* Gradual turn-on of output transistors by splitting the output in multiple stages
* Dynamic smoothing circuit by softening the turn-on to obtain gradual takeover of current (di/dt control)



OEC is a trademark of Texas Instruments Incorporated

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Signal slew rate improvements seen in Advanced Logic circuits have mainly been achieved through clever circuit output stages. These innovative output stages assure that the change in output current (di/dt), and correspondingly the change in output voltage (dv/dt), are controlled.

This advanced technique developed by Texas Instruments is called :

Output **E**dge **C**ontrol (OEC™)

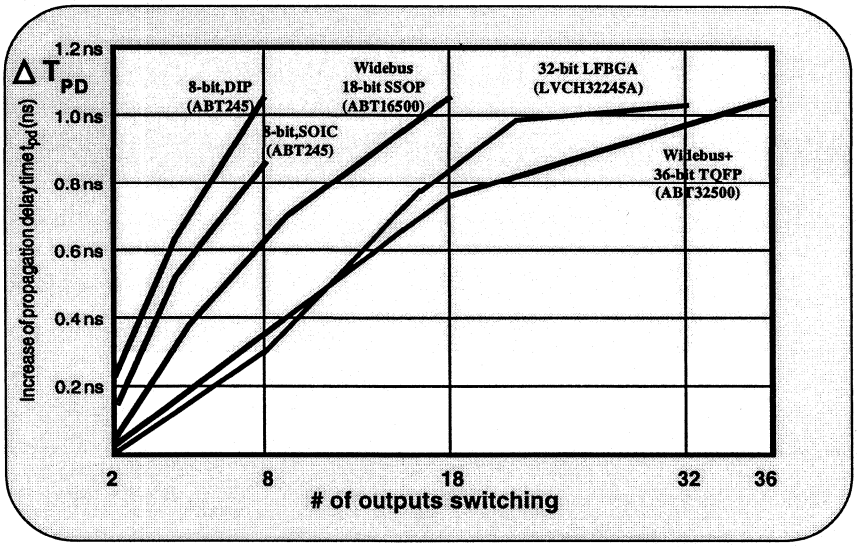
The use of parallel output transistors that are turned on one after the other limits the signal slew rate.

A side effect is that the output noise levels are almost independent of the circuit load.

This OEC on the output stage has been implemented in the following three 5V families : AC, AHC and ABT and in all advanced low-voltage families .

Digital Design Seminar

ΔTPD vs Number of Outputs Switching



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The propagation delay of the component also depends on the number of simultaneously switched outputs.

The reason is that **the inductance of the supply leads acts as a "current brake"** .

For devices in conventional packages (DIP and SOP) an additional delay of 150 to 200 ps for each output switched needs to be taken into account.

For example, an SN74F244 will have a maximum delay t_{pHL} = 7.5 to 8 ns, if all eight outputs switch simultaneously.

In this respect, the **multiple V_{CC} leads in Widebus™ circuits are of advantage.** They may not eliminate the effect, but at least they ensure that the loss of speed is no greater than in octal bus drivers, even though twice as many outputs are switched.

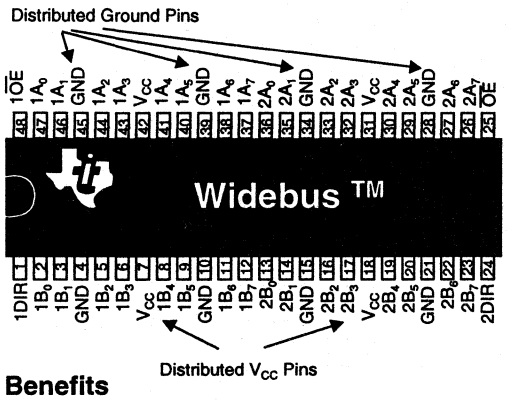
The newest Logic package available from TI is the **Low-Profile Fine Pitch BGA (LFBGA) package.** Through reduced lead inductance and overall improved electrical performance, one can see from the graphic above that even when switching 32 bits, the delay is the better than the SSOP package switching almost half the number of bits.

Digital Design Seminar

Widebus™ / Widebus+™ Devices

Reduce Component Count

'16245 Widebus Package Pin-out



TI Logic devices available in Widebus™

Family	16 Bits	18 Bits	20+ Bits	
ABT	25	20	14	
AC/T	15	4	3	
AHC/T	7			
LVC	16			
ALVC	20	19	24	
LVT	19	11	3	
ALVT	25	6	10	
*AVC**	*8*	*3*	*5*	*(Planned)*

Benefits

- √ Improved Noise Performance
- √ Significant Speed Improvement
- √ Saves Production Time

Widebus is a trademark of Texas Instruments Incorporated

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Widebus™ circuits offer designer substantial advantages when it comes to designing advanced systems.

With the growing performance demands that are being made of computer systems, one has to expand the width of bus systems to 16 or 32 bits, so that high data throughput can be achieved. As the available space for a circuit is limited, this can only be implemented with components like Widebus™, which support wide bus architectures at an attractive cost.

As circuits become faster, the electrical characteristic of the package becomes more and more the focal point. Besides the unavoidable lead capacitance, it is primarily their inductance that determine the response of fast digital circuits and which, in some cases, limit their usage.

In addition, doubling the transfer channels in the new circuits reduces the component count by 50%.

Each of these new components is no bigger than a conventional 24-pin SO package, as the new circuit uses only 50% of the area previously used.

TI offers more than 210 Widebus™ functions.

The excellent electrical behaviour of Widebus™ packaging is used for devices operating from 5V and 3V supply voltage.

For 5V families TI offers ABT and AC as well as some functions in the AHC family.

For 3.3V supply voltage Widebus™ devices are available in AVC, LVC, ALVC, LVT and ALVT with many more planned for ALVT and AVC.

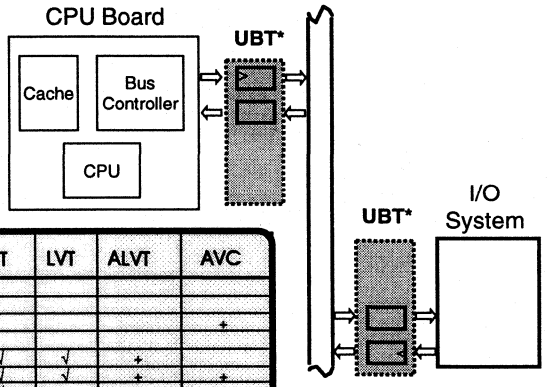
Widebus+™ supports up to 36 bits within one single package.

Digital Design Seminar

Universal Bus Transceivers

A flexible Bus Interface Concept

* UBTs can replace nearly all common bus interface logic parts ('245, '543, '2952, etc.)
* Clocked storage "out"
  Latched or Transparent "in"
* Shortens time to market with common t_{su}, t_h and min delay times



Device	UBT™ Part Description *	ALVC	ABT	LVT	ALVT	AVC
'16409	9-Bit Non-Inverting 4-port UBE	√				
'162409	9-Bit Non-Inverting 4-port UBE with series resistor	√				
'16334	16-Bit UBT	√				+
'162334	16-Bit UBT with series resistors	√				
'16500	18-Bit Non-Inverting UBT	√	√	√	+	
'16501	18-Bit Non-Inverting UBT	√	√	√	+	+
'16600	18-Bit Non-Inverting UBT	√	√		+	
'16601	18-Bit Non-Inverting UBT	√	√		+	+
'32501	36-Bit Non-Inverting UBT		√			+
'32316	16-Bit Non-Inverting 3-port UBE		√			
'32318	18-Bit Non-Inverting 3-port UBE		√			
162500	18-Bit UBT with series resistors		√		+	
162501	18-Bit UBT with series resistors		√		+	
162601	18-Bit UBT with series resistors	√			+	
'16901	18-Bit Non-Inverting UBT with Parity Gen./Chk	√			+	
'16282	18 to 36-Bit Registered Bus Exchanger	√				
'162836	20-Bit Universal Bus Driver with series resistors	√				

*UBT is a trademark of Texas Instruments Incorporated

+ planned

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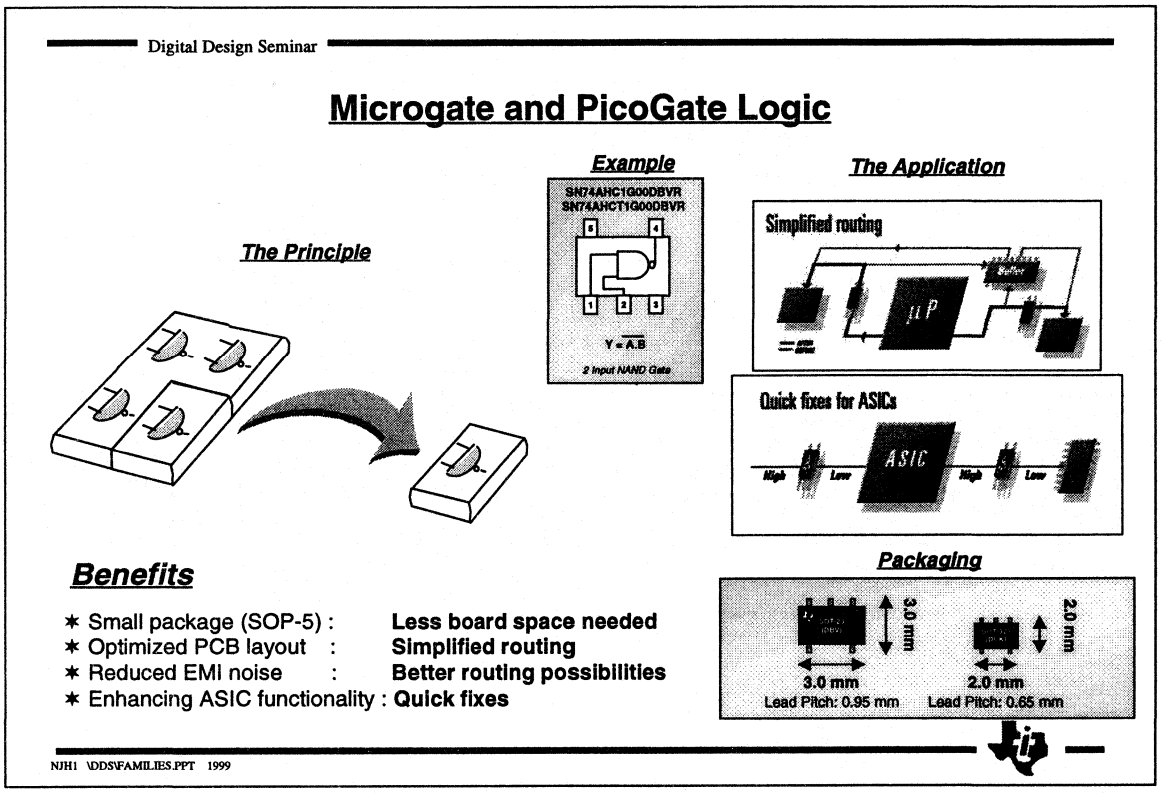
Many high performance applications require more than one mode for accessing their system bus, because different parts of the system have different data access and processing speeds. While some may be able to work in transparent mode (fully synchronous to the data source), others will require data to be latched, to meet setup and hold time requirements. When designing CPU access to the bus, clocked storage is the easiest method.

UBT™'s are bi-directional transceivers that can be configured as :

- Transparent,
- Data-flow-through transceivers (e.g. '245 function),
- Latch-enabled transceivers (e.g '543 function) ,
- Clocked registered transceivers (e.g. '646 function),
- And clock-enabled registered transceivers (e.g. '952 function).

Designed specifically for workstation bus-interface applications, the UBT™ is perfect as an interface to many different microprocessor architectures and system backplane specifications available. It may also be cost effective in low volumes as an alternative to several different interface functions.

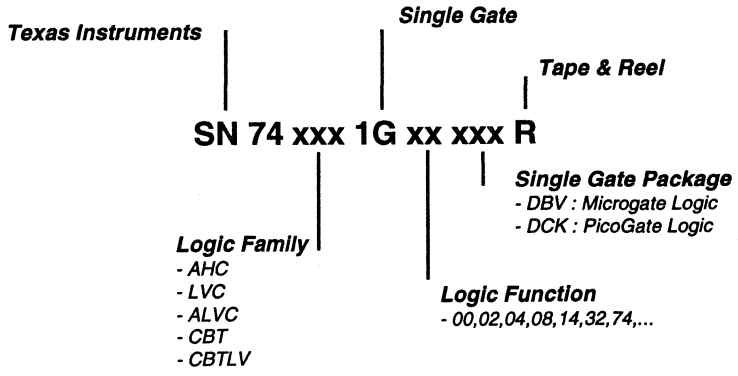


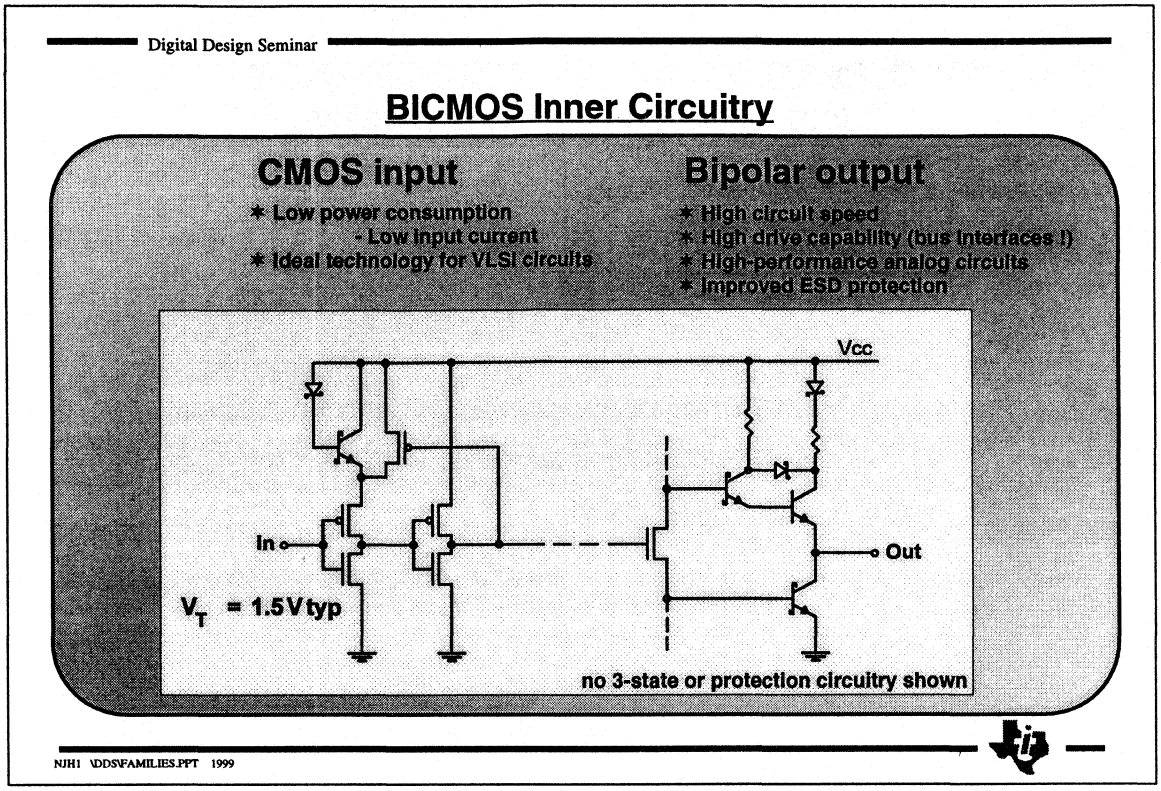
Microgate's five-pin SOP-5 package is the same size as the well known Small-Outline Transistor (SOT-23) package, which features a 0.95 mm lead pitch and is 1.3mm high, whilst PicoGate Logic is one of the smallest integrated circuits in the industry and has a 0.65 mm lead pitch and is only 1.0 mm high.

Microgate Logic and PicoGate Logic allow the designer to place a particular gate function in close proximity to related circuitry, shortening and simplifying the routes on a board, and so optimizing the EMI performance of the system.

As systems evolve, a designer can alter an output of an ASIC without re-designing and manufacturing an entirely new ASIC. This can extend the useful life of an ASIC design as well as maximize the return on investment the system vendor has made in such a device. In addition, rather than redesigning an ASIC, Microgate and PicoGate Logic devices can be used to correct minor flaws in ASIC designs.

Single Gate nomenclature can be seen by the example below:





By combining elements of both bipolar and CMOS circuits on a single silicon chip, BiCMOS is able to provide speeds equivalent to existing advanced bipolar solutions with 90% less power consumption. From a power (current) consumption standpoint, bipolar output stages provide the following two advantages:

1) Lower voltage swing than a CMOS output. The power used when charging or discharging the internal circuit capacitances and the external load capacitance is reduced.

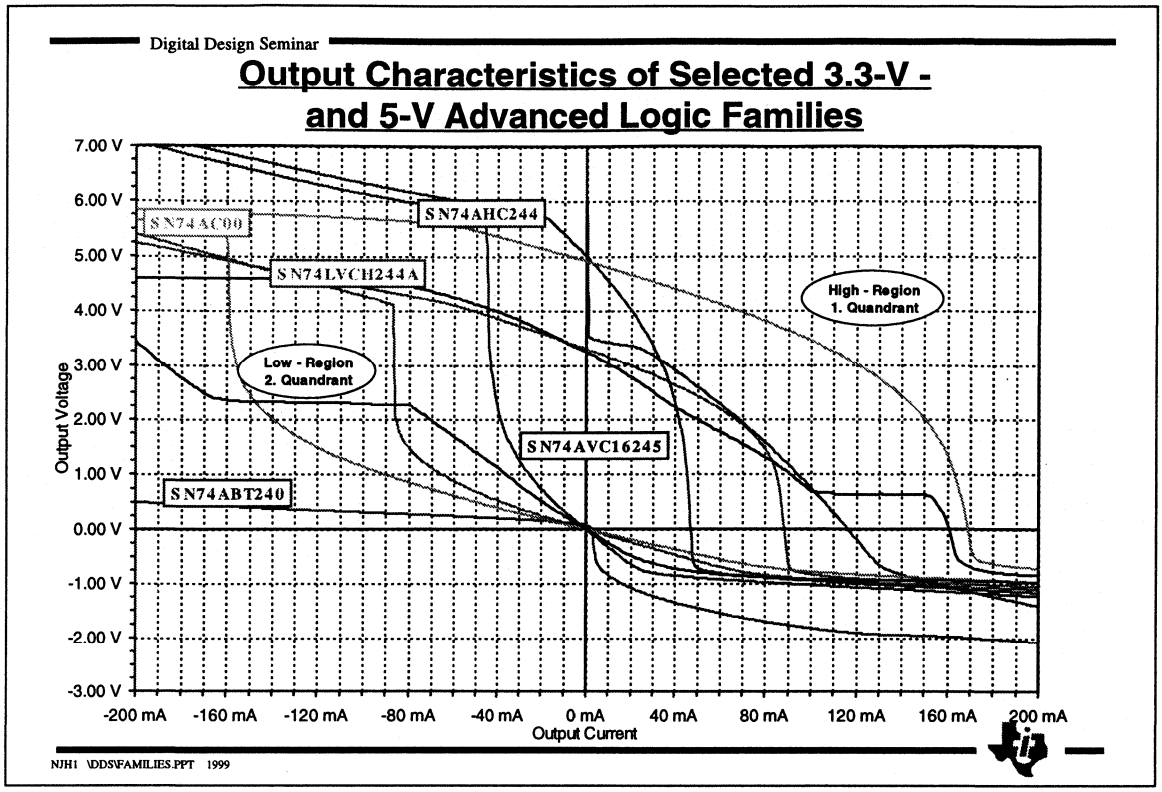
2) The bipolar transistors are capable of turning off more efficiently than CMOS transistors. The wasteful flow of current from V_{CC} to GND is reduced.

Although bipolar tends to have a high static power consumption, its lower dynamic power consumption allows for better overall power performance at high frequencies than either pure bipolar or CMOS as the dynamic power makes up most of a device's overall power consumption.

Simplified input and output stages of an BiCMOS transceiver are shown on this slide. As these inputs are implemented in CMOS circuitry they offer high impedance for low leakage and low capacitance for minimum bus loading.

BiCMOS outputs use bipolar circuitry to provide the speed and drive necessary for a bus interface. A major advantage of this output stage is the reduced voltage swing, which lowers ground noise, improves signal integrity and reduces dynamic power consumption.

Because of its small process geometry, tight metal pitch and shallow junctions, ABT can provide for strong output drive currents (sink current 64mA, source current 32mA) and low capacitances. As a result of these enhancements, internal propagation delay is very low, and the devices show good behaviour regarding noise.



The curves show the drive capability in the logic HIGH and LOW - states for various 5V and low-voltage logic families.

The steeper the HIGH- (LOW-) curve, the higher the drive capability.

Note! : **ABT** is a BiCMOS family and delivers, when supplied with 5-V, TTL levels at the outputs (typical output high: 3.6 V).

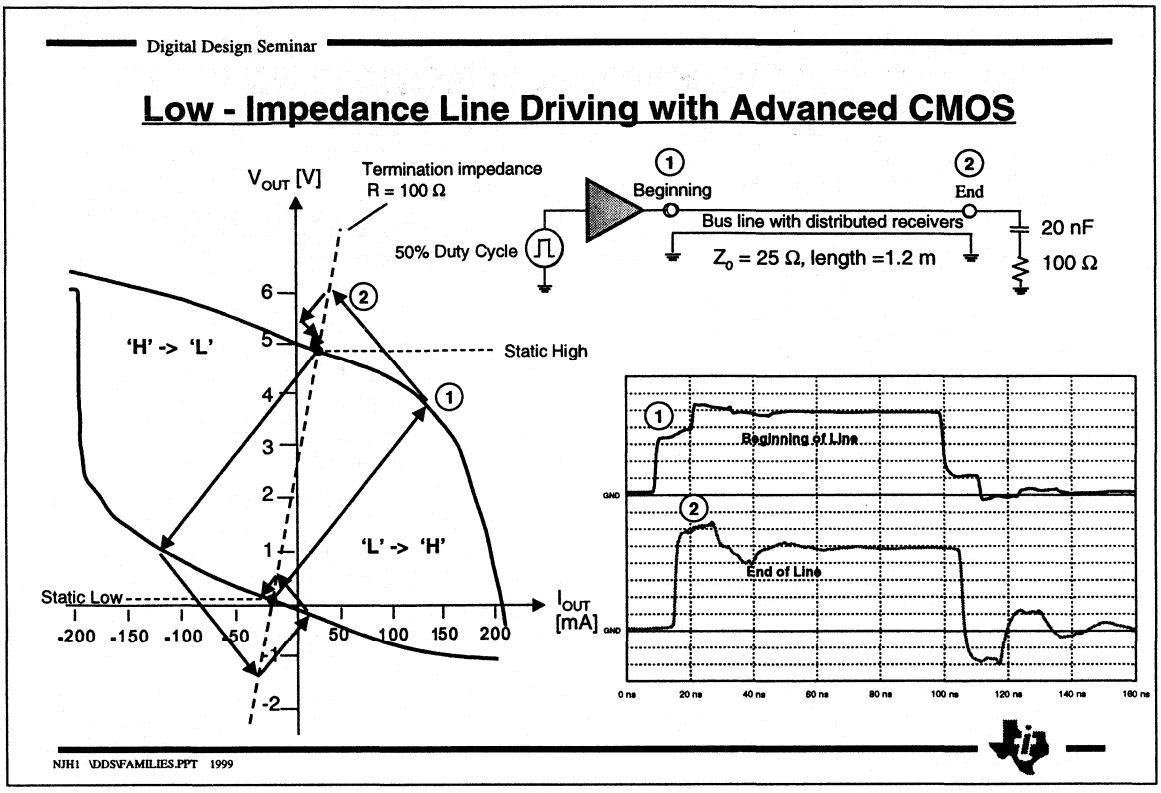
LVC and AVC are supplied with 3.3 V, thus the high characteristic shows a maximum output voltage of 3.3 V

These characteristic curves can be taken as base for the graphical calculation of over- and undershoots of a given family.

For the Bergeron method, as mentioned earlier, two extra physical parameters are necessary:

- The **line impedance**
- The value of the **line termination resistor**.

An example is given on the next page.



As an example of the graphical Bergeron method, a low impedance line is evaluated.

The set up is as follows:

A line driver AC is connected to a line which impedance is Z_O = 25 Ohm, the length of the line being 1.2 m. The line is terminated with 20nF in series with 100 Ohm. The generator delivers a digital signal with 50% duty cycle.

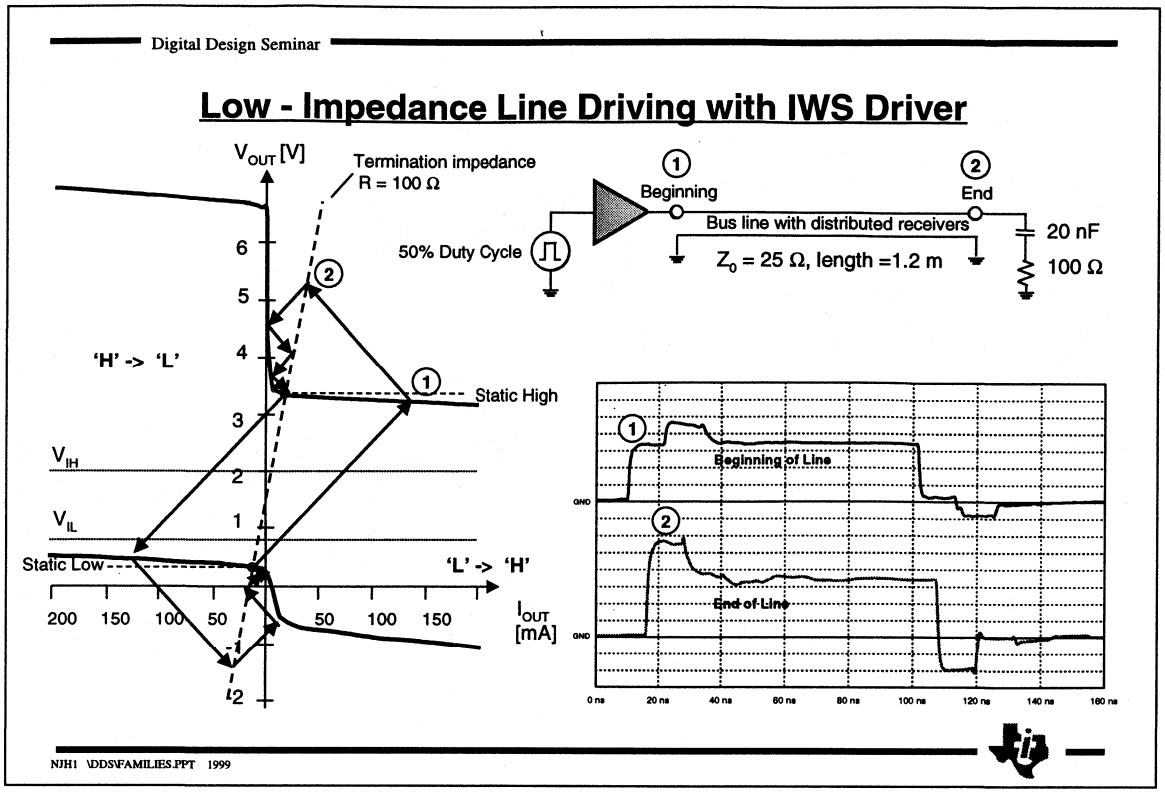
The first step to solve this problem graphically is to choose the output characteristics of the AC driver.

The termination resistor of the setup together with the duty cycle (50%) results in the dashed straight line. The line impedance (Z_0) results in the steepness of the progressing waves (solid arrows).

Each crossing of the output characteristic and the solid arrow can be recognized as a voltage value at the beginning of the line (Output driver).

Each crossing of the termination curve and the solid arrow can be recognized as a voltage value at the end of the line (termination resistor).

Using an AC driver for low line impedance may generate the problem that the beginning of the line achieves with the incident wave only a value slightly above 3V. Therefore one has to wait for the reflected wave to see the valid CMOS high level which is 70% of V_{CC}.



For the same set-up as before, but with the line impedance decreased further down to 20 Ohms, the Bergeron method is applied, using an ABTH25245, an Incident Wave Switching (IWS) driver instead of the AC driver.

The graph shows that again with the first wave, a change of the logic level is easily ensured. The beginning of the line is directly switched to either logic HIGH or logic LOW.

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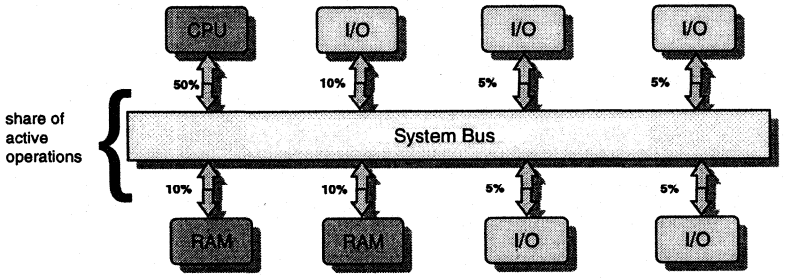
Static Power Consumption
Application Example



5 V				Application	3.3 V					
74F245	ALS245	ABT245	AHC245	Family	AVC16245	ALVTH16244	LVT245	LVC245	ALVC245	LV245
107.5 mA	35.5 mA	7.69 mA	0.04 mA	1 x Icc(50%)	0.04 mA	1.32 mA	1.39 mA	0.01 mA	0.02 mA	0.02 mA
328.5 mA	112.5 mA	5.21 mA	0.12 mA	3 x Icc(10%)	0.12 mA	1.00 mA	1.29 mA	0.03 mA	0.06 mA	0.06 mA
439.0 mA	151.0 mA	3.98 mA	0.16 mA	4 x Icc (5%)	0.16 mA	0.85 mA	1.24 mA	0.04 mA	0.08 mA	0.08 mA
875.0 mA	299.0 mA	16.88 mA	0.32 mA	Icc Total	0.32 mA	3.17 mA	3.93 mA	0.08 mA	0.16 mA	0.16 mA
5 V	5.0 V	5.0 V	5.0 V	Vcc	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
4375 mW	1495 mW	84.4 mW	1.6 mW	Power	1.1 mW	10.5 mW	13.0 mW	0.26 mW	0.53 mW	0.53 mW
51.85	**17.72**	**1.0**	**0.02**	**Factor (Vxl)**	**0.013**	**0.124**	**0.154**	**0.003**	**0.006**	**0.006**
7.0 ns	7.5 ns	3.6 ns	6.5 ns	tpd max	1.7 ns	2.4 ns	3.5 ns	6.3 ns	3.0 ns	10.0 ns

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This foil shows an application example in a computer system.

CPU, RAM and I/O ports are connected via a bus. The percentage value shows the share of activity on the bus (e.g. the CPU uses the bus for 50% of the time). If we assume that all components used for this application are taken from the same family and we set up four identical systems, we can compare the performance.

The **74F family** uses the highest power consumption for the application. This family is made in bipolar technology and consumes in tri-state the same current as during active operation. Also the propagation delay time is the slowest with 7 ns.

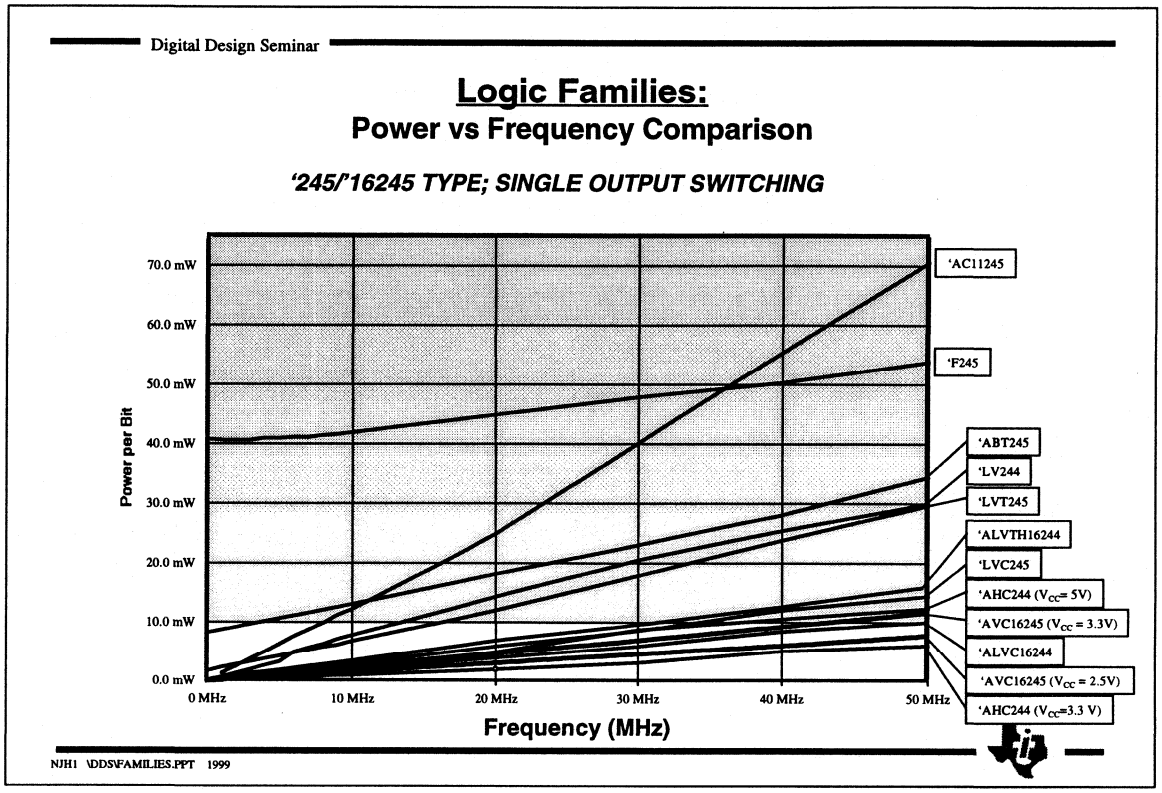
ABT has improved performance in both power consumption and speed. ABT devices are made in BiCMOS Technology. During tri-state mode the power consumption is decreased down to 190 mA. The speed is increased by 44% against the 74 F family.

A comparison with **ALVC** shows that only 1.3% of the ABT power consumption is used by ALVC. Also the propagation delay is improved to a value of Tpd=2.9 ns.

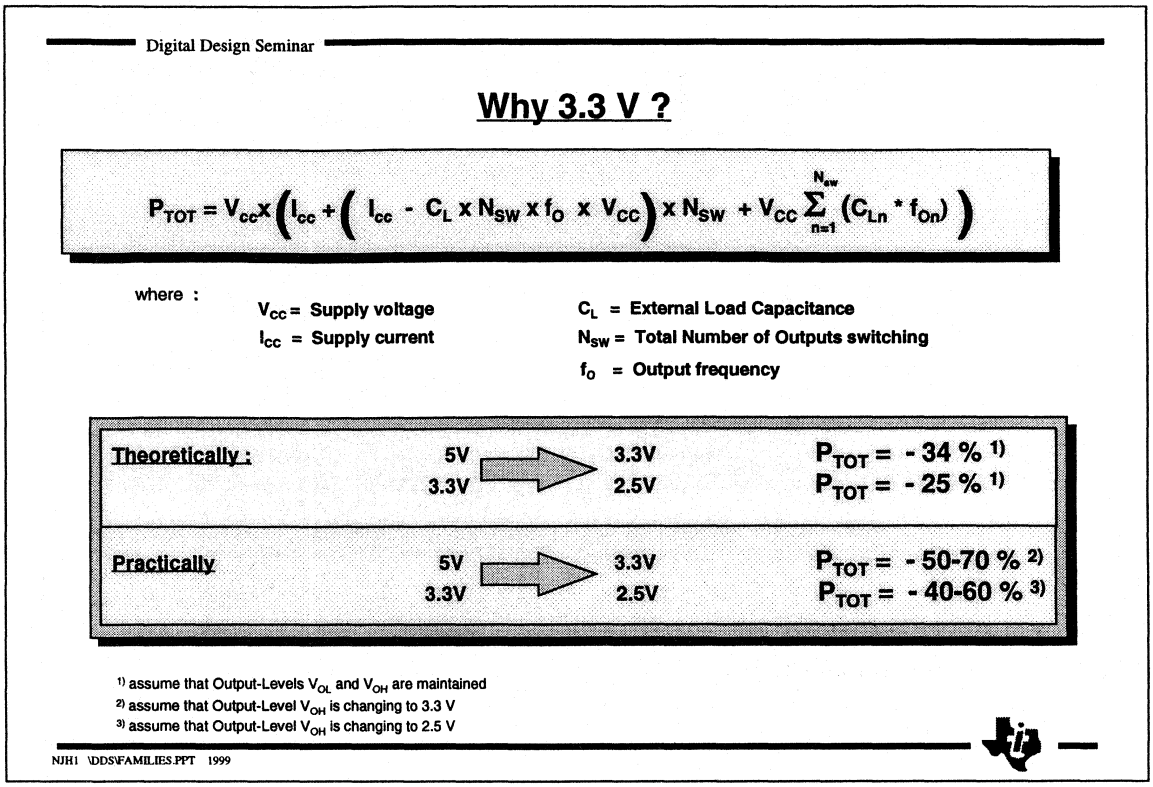
One can easily see that **LVC** has the lowest power consumption (0.3% of ABT power) of all the low-voltage families.

ALVT is the fastest BiCMOS technology described here and has even less power consumption then LVT.

The fastest standard logic family available from Texas Instruments at the moment is **AVC**. Given the performance of this family, it still has very low power consumption compared to the other slower families.



This foil shows the dynamic power consumption of different 5V, 3.3V and 2.5V optimised Logic families from Texas Instruments.



The answer to the question : "**Why 3.3V**" is given by the formula for determination of the power consumption related to logic circuits, here as an example the formula for CMOS devices (CMOS level inputs) .

A logic circuit's total power consumption, P_{TOT}, is strongly influenced by a number of parameters. If we investigate this formula, we can split this into two parts:

1) V_{CC}

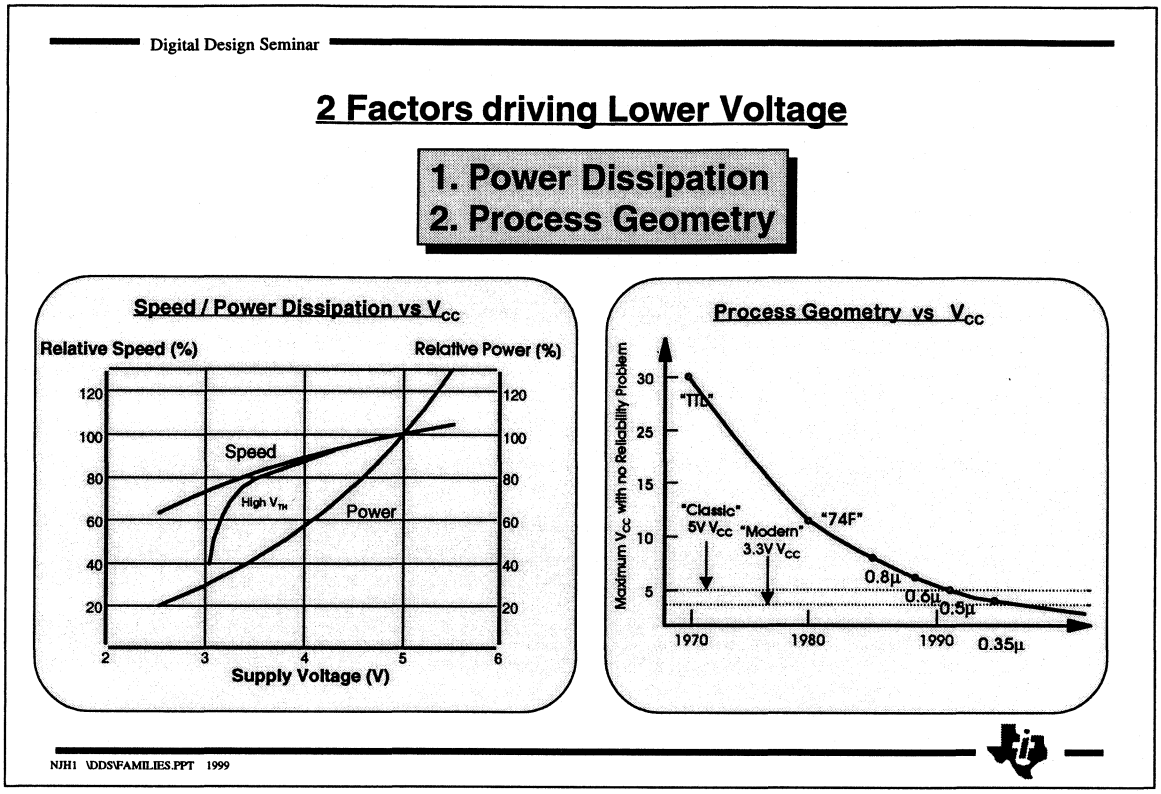
2) the 'rest' , which is determined by various parameters such as number of outputs, frequency, etc.

Some are inherent to the technology, like the **static I_{CC} currents** and the so-called **"current spike"**, that flows across the output during circuit switching. Others depend on load conditions, operating frequency, and so on.

However, the **parameter with the most significant effect on the overall power consumption is V_{CC}**.

The theoretical saving on power dissipation is 34%, if you reduce the voltage from 5V down to 3.3V and the theoretical saving on power dissipation is 25%, if you reduce the voltage from 3.3V down to 2.5V

Practically, the power saving will be about 50-70% for 3.3V and 40-60% for 2.5V supply voltage, because other parameters are also improved by reducing the supply voltage.

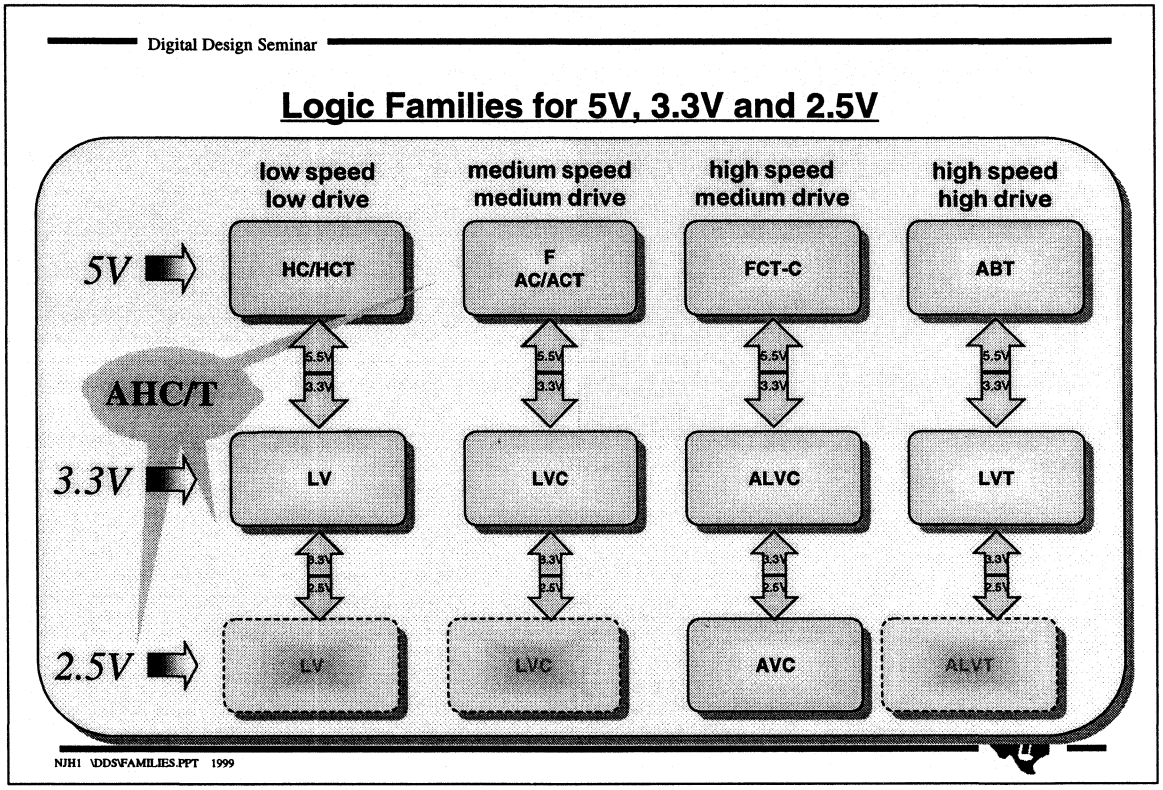


Changing a system's V_{CC} from 5V to 3.3V by reducing a circuit's supply voltage will worsen its speed. However, as the figure on the left shows, the **relative loss of speed is much less than the improvement in power consumption**.

Practically, most system designs do not allow for any speed degradation. The way out for suppliers is to use process technologies with smaller feature sizes that compensate (or even overcompensate) the speed loss. This results in the availability of 3.3V logic families that offer the same or higher speeds than the 5V families they replace, in combination with a drastic reduction of the power consumed.

The significant improvement in power consumption is only one reason why there is such a strong momentum in the industry to migrate towards reduced supply voltages.

Another strong push to reduce V_{CC} is driven by the **accelerated use of small process geometries**. Advanced microprocessors or ASICs sometimes employ several millions of transistors. This demands process feature sizes of 0.5 micron and below. Unfortunately, such small process geometries start to show reliability problems if operated with a 5V supply voltage. Some types of equipment, e.g. industrial control systems, are therefore frequently forced to change their V_{CC} to 3.3V, although their operating environment would still allow for the high power consumption of 5V designs.



Texas Instruments' Low Voltage Logic families have been designed to provide a performance that is at least equivalent to, but usually even better than, that of commonly used 5V devices.

If you are in the situation to design a new application with 3.3V logic, but are only familiar with the performances of the 5V logic families, this foil will help you.

LV is rather like the well-known LS and HC/HCT families, but features improved speed.

LVC addresses the medium performance range, where families like F or AC are predominant in 5V applications.

Two different solutions are available for high performance 3.3V system design:

ALVC combines medium output drive with very high speed performance (unmatched by any other 3.3V logic family).

AVC together with the TI's DOC™ circuit, is optimised for 2.5V and is the natural migration family for ALVC

LVT, which is the 3.3V equivalent to the 5V ABT family of bus interface devices, combines speed with a drive capability that is high enough for reliable operation of large backplanes.

ALVT, which is the upgrade to the 3.3 LVT family of bus interface devices, combines higher speed with a same drive capability. ALVT is also specified down to 2.5V.

There is also a migration path showing potential equivalent families for 2.5V operation. Most families will work at a lower voltage node, but will function with reduced speed and drive.

TI will continue to design and release logic families that will provide optimised migration paths to 2.5V (AVC newest family) and below.

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Texas Instruments 3.3V CMOS Logic Technical Comparison

Product Family	SN74LV245 @ 3.3V	SN74LVC16245 @ 3.3V	SN74ALVC16245 @ 3.3V	SN74AVC16245 @ 3.3V
Speed (typ/max)	5.9ns/10ns	-/4.0ns	2.1ns/3.0ns	-/1.7ns
Drive (IOH/IOL)	-8mA/8mA	-24mA/24mA	-24mA/24mA	-12mA/12mA (Static)
Current Consumption	ICCH/Z = 10µA	ICCH/Z = 20µA	ICCH/Z = 40µA	ICCH/Z = 40µA
Power-off Leakage Current				
IOFF	±5µA	±10µA	-	±10µA
Interface Capability	Mixed Mode	Mixed Mode	Pure 3.3 V	Mixed Mode
	5V Tol. I/O	5V Tol. I/O	-	3.3V Tol. I/O
Vcc Range	2.0V - 5.5V	1.65V - 3.6V	2.3V - 3.6V	1.65V - 3.6V
Switching Noise	Ground-Bounce less than 800 mV			
Temperature Range	-40 to +85 Degrees Celcius			
Package	SOIC/SSOP/TSSOP	SOIC/SSOP/TSSOP/TSSOP/ LFBGA/SOT-5	SSOP/TSSOP/TSSOP/ LFBGA/SOT-5	SOIC/SSOP/TSSOP/TVSOP LFBGA/SOT-5
Price Similarity	~HC	~AC	~FCT	-
Special Features				
I/O Tolerance	5V	5V	-	3.3 V
BusHold	-			-
Dampling Resistors Option	-			DOC Circuit
Additional Specification	2.5V and 5V	1.8 and 2.5V	2.5V	1.8V and 3.3V
Live Insertion	-		-	
			SG/Gates/Octals	
			Also specified @ 1.8V	
Cross-Reference	Philips : 74LVxxx	Philips : 74LVCxxx	Philips : 74ALVCxxx	Philips : 74AVCxxx
	Hitachi : HD74LV	Hitachi : HD74LVCxxx	Hitachi : HD74ALVCxxx	
		IDT : 74LVCxxx	IDT : 74ALVCxxx	
		Fairchild : 74LCXxxx		
		Motorola : MC74LCXxxx		
		Toshiba : TC74LCXxxx		

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These **three optimised 3.3-V and one 2.5V optimised (AVC) CMOS logic families** can be used for portable applications from electronic games up to high performance engineering workstations.

The **LVC** and the **LV** families are designed for low cost 3V systems such as consumer equipment, portable computers, electronic games, toys and portable telecom equipment that require medium performance at low cost. They are so-called bridge families. Their 5V tolerance supports mixed voltage operations.

The **ALVC** family, with a typical propagation delay time of 2ns has been designed to meet the requirements of high speed systems including engineering workstations and interfaces to SDRAM-modules.

The **AVC** family is the newest member to the Texas Instruments Logic portfolio and boosts an incredible 1.7ns tpd(max) at 3.3V and even a sub-2ns propagation delay time at 2.5V through its revolutionary DOC™ circuit. This family also features 3.3V tolerance for mixed-voltage operation.

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Texas Instruments 3.3V BiCMOS Logic Technical Comparison

Product Family	SN74ALB16245 @ 3.3V	SN74LVTH16245 @ 3.3V	SN74ALVTH16245 @ 3.3V
Speed (typ/max)	1.3ns/2.0ns	2.3/3.3ns	-/2.4ns
Drive (IOH/IOL)	-25mA/25mA	-32mA/64mA	-32mA/64mA
Current Consumption	5.6 mA / Buffer	ICCH/Z = 190µA	ICCH/Z = 100µA
		ICCL = 5mA	ICCL = 4.5mA
Power-off Leakage Current			
IOFF	-	±100µA	±100µA
Interface Capability	Pure 3.3 V	Pure 3.3 V	Mixed Mode
	-	5V Tol. I/O	5V Tol. I/O
Vcc Range	3.0V - 3.6V	2.7V - 3.6V	2.3V - 3.6V
Switching Noise	Ground-Bounce less than 800 mV		
Temperature Range	-40 to +85 Degrees Celcius		
Package	SSOP/TSSOP	SOIC/TSSOP	SSOP/TSSOP/TVSOP
Price Similarity	~ABT	~ABT	~LVT
Special Features			
I/O Tolerance	-	5V	5V
BusHold	-	√	√
Dampling Resistors Option	-	√	√
Additional Specification	-	-	2.5V
Live Insertion	-	√	√
Auto Tri-State	-	-	√

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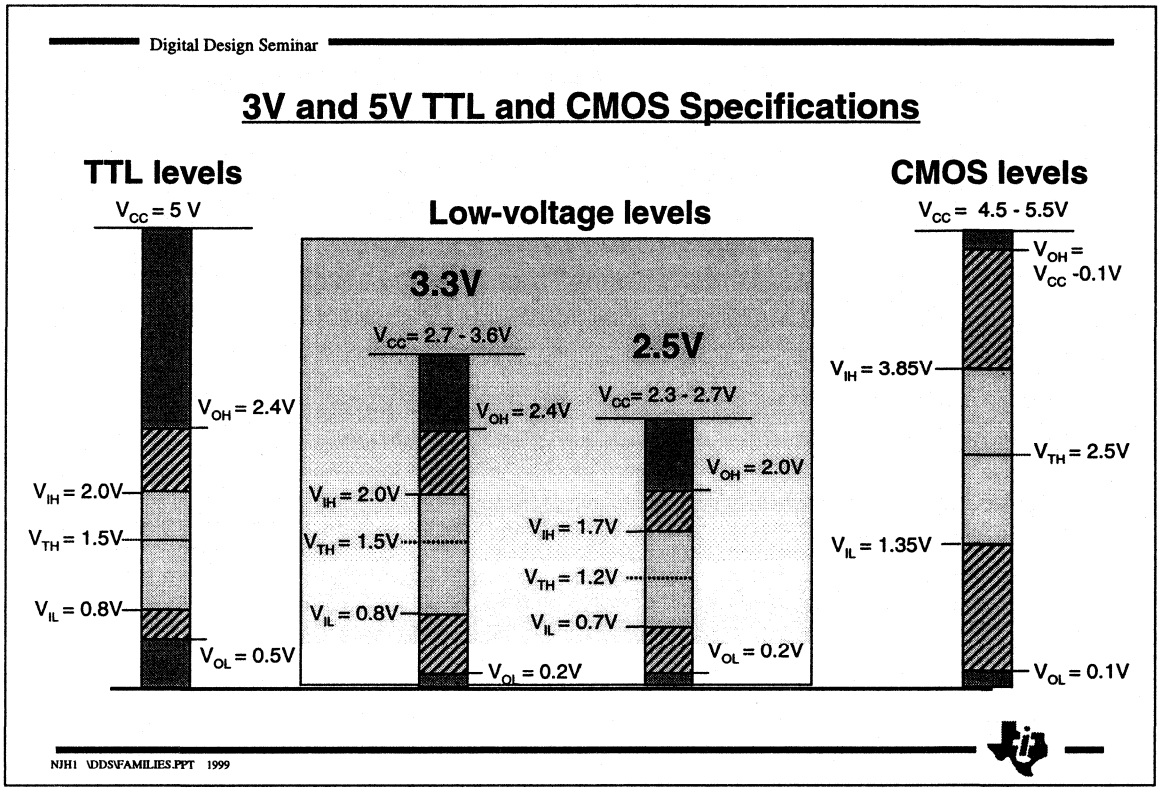
These **three 3.3-V BiCMOS logic families** with their high drive capability, can be used for Backplane/Bus driving applications, high-performance engineering workstations, desktop PC's and telecom transmission/switching equipments.

The **LVT** and **ALVT** families are so-called bridge families. Their 5V tolerance supports mixed voltage operations.

The **ALB** (Advanced Low Voltage BiCMOS) family is the fastest Logic family in the TI low voltage logic portfolio. There are two devices available, the SN74ALB16244 and SN74ALB16245, which are intended to replace the conventional bus drivers in any speed-critical path.

Handheld systems have to be light and small (e.g. mobile phones). This is why the package range of low power logic includes only advanced package options (SOIC,SSOP,TSSOP,TVSOP) .

TI has second source agreements with Philips and Hitachi for Low Voltage Logic families. The agreement with Philips has recently been extended to cover other new logic families such as ALVT and AHC.



Before discussing the special requirements of mixed mode designs (i.e. systems where there is a need to interface between 5V, 3.3V and 2.5V), we would like to briefly discuss the different voltage level specifications used in both environments.

During the development of the 3.3V and the 2.5V switching specification in JEDEC, there were basically two "interest groups" endorsing slightly different proposals.

The LV-CMOS proposal was mainly targeted to mobile applications, where battery operation requires a V_{CC} min of 2.7V.

This proposal favoured a concept that basically copied the 5V CMOS one, i.e. an output voltage swing that almost equals V_{CC}, where V_{OL} ~ 0V and V_{OH} ~ VCC. This would allow the proper operation of existing 5V CMOS devices from 3.3V ("Scaled CMOS").

On the other hand, the LV-TTL proposal favoured V_O/V_I specifications that are identical with 5V TTL, so that interfacing the two worlds is greatly eased.

Fortunately the final 3.3V specification agreed upon by JEDEC covers both proposals.

It specifies a 2.7-3.6V V_{CC} range, in which the max/min values of the logic input levels are identical with the 5V TTL spec (0.8/2.0V) and max/min values of the logic output levels match the CMOS spec.

Additionally, JEDEC has also now a specification for 2.5V switching levels, as shown above.

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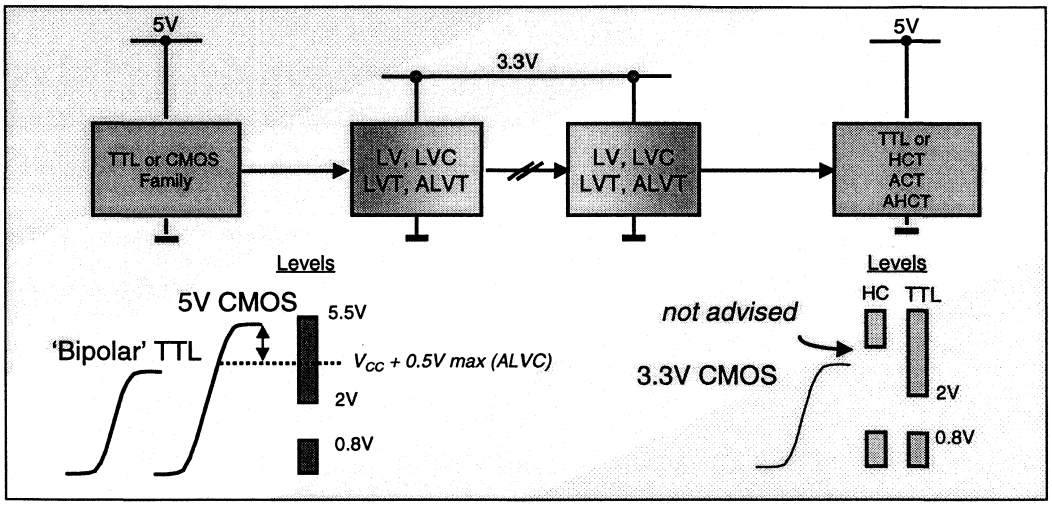
5 Volt 3.3 Volt Interfacing:
LV, LVC, ALVC, LVT and ALVT



* **LV, LVC LVT and ALVT** devices allow **direct interfacing** from 5V TTL and 5V CMOS devices (5V tolerance)
* **ALVC** input levels can only go V_{CC} + 0.5V max
* Direct interfacing from 3.3V levels to 5 V CMOS is not advised

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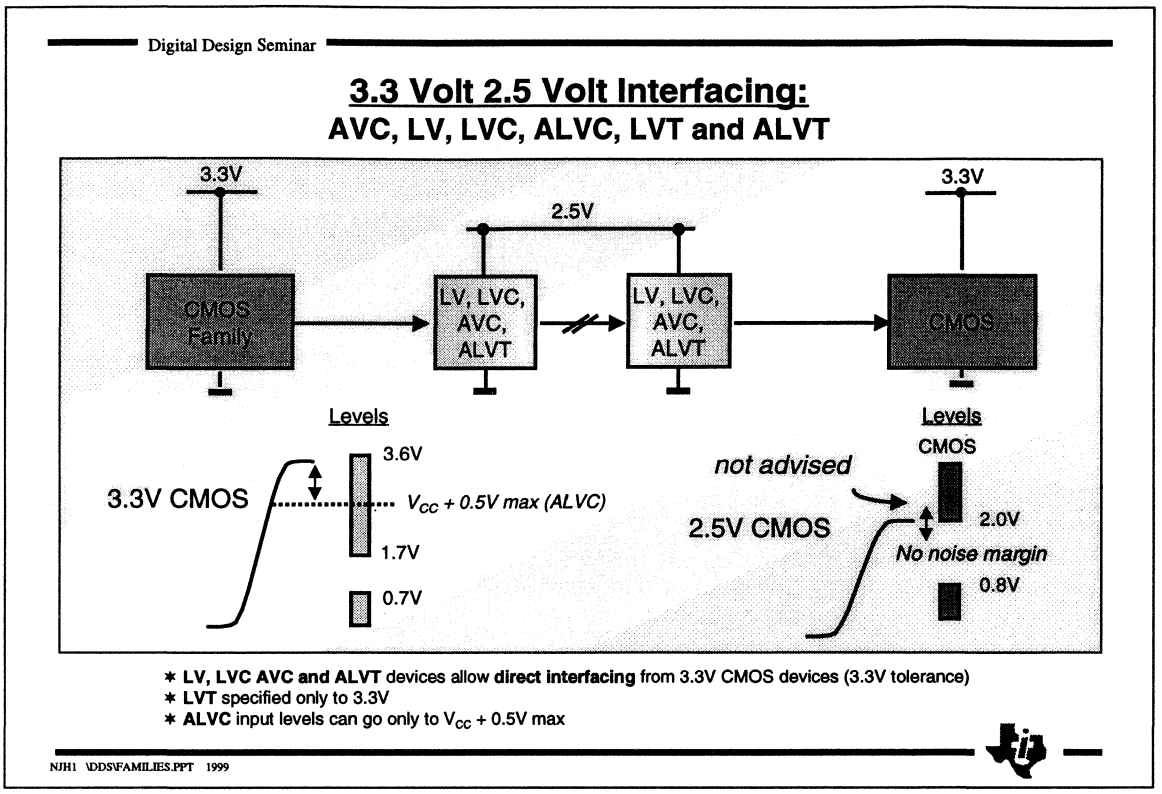
As has been seen from this page, ALVC does not have 5V tolerance.

However, this does not necessarily mean that this family is unable to interface with 5V signals.

If a 5V TTL signal is applied, its high level will typically be about 3.2V. This does not violate the ALVC inputs specifications. One must make sure, however, that no overshoots will occur on the line which might again cause trouble.

On the output side, **all low-voltage families can directly drive 5V inputs that are TTL-compatible**. No additional provisions have to be made.

If the 5V receiver expects to see CMOS levels a special 'Level-Shifter' is required.

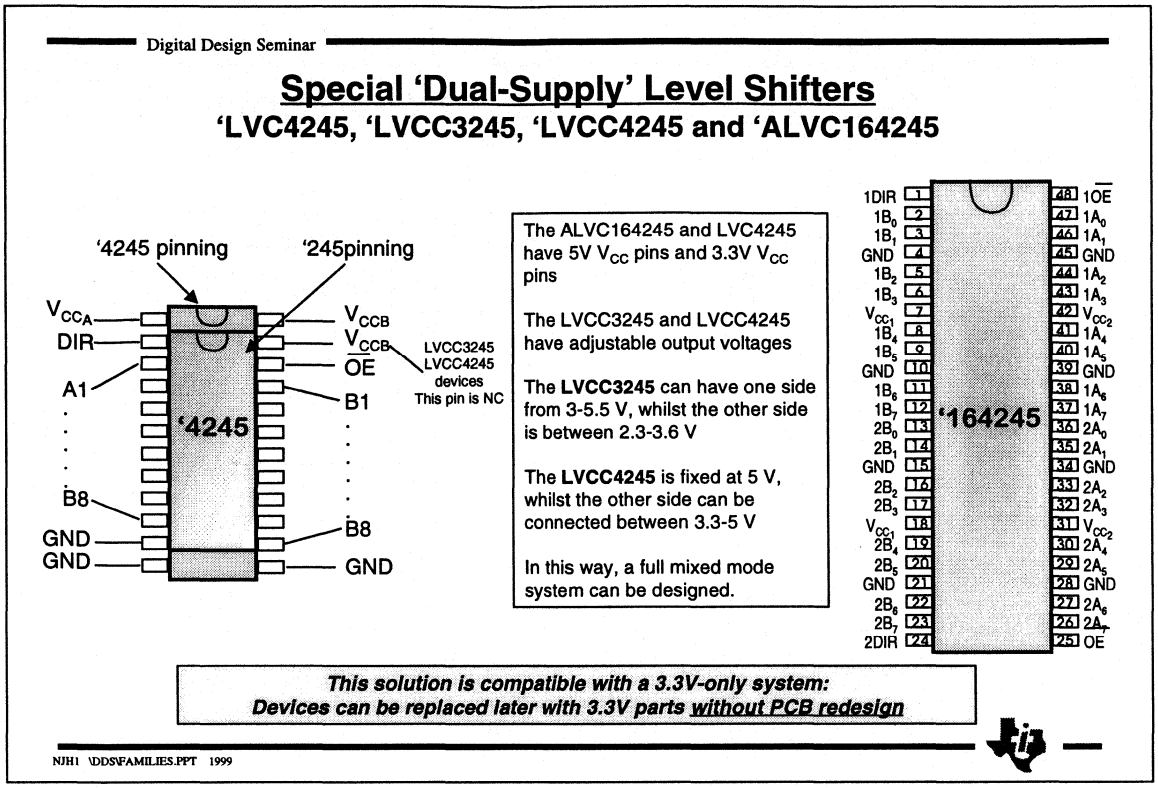


Again here, ALVC does not allow voltages higher than V_{CC} + 0.5V. This means that with a 3.3V CMOS voltage swing, the input level will be violated, since V_{CC} is 2.5V.

In this case, this family is unable to interface with 3.3V signals.

On the output side, the typical output voltage of a 2.5V CMOS device is about 2.0V. This happens to also be the input switching level for 3.3V LVTTL levels. This means that in theory, the **LV, LVC, AVC and ALVT families could drive a 3.3V CMOS input**, however, this is not recommended, since there is absolutely no noise margin.

In order to guarantee that the 3.3V input will accept the 2.5V CMOS level, a level shifter must be used to raise the voltage level to the correct 3.3V switching levels.



Certain applications will require a 'Level-Shifter' between 2.5V, 3.3V and 5V to provide 3.3V and 5V output signals. Examples are:

1) Interfaces from a 2.5V ASIC to 5V I/O modules.
2) Interfaces to 5V CMOS-level devices which, as shown on the previous page, cannot be operated reliably from 3.3V outputs.
3) 5V memory modules that must be connected to 3.3V components.

In the latter case a designer might want to provide a true 5V input signal to the memory, even if it has a TTL-type input, as the memory circuit's current consumption will otherwise be increased.

In these cases, a **dual V_{CC} level shifter** will be required. These are device where the supply voltages V_{CCA} and V_{CCB} can be connected to a variety of different voltages ie. 2.5V, 3.3V and 5V and the device will shift the inputs voltage levels to the necessary output levels for the receiving device.

Here are **four level shifter examples**. The LVC4245, LVCC3245, LVCC4245 are octal level-shifters and the ALVC164245 is a 16-bit level-shifter

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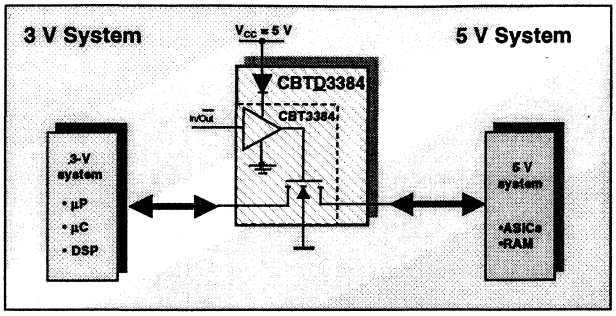
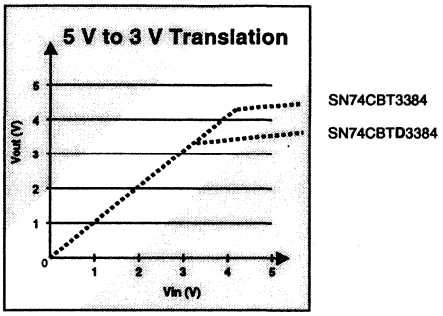
SN74CBTD3384 for 5 V to 3.3 V translation





★ Crossbar Switches (CBT) with integrated diode (SN74CBTD)

★ 250 ps switching speed

★ Bi - directional level translation : 5V TTL ⇔ 3.3V LVTTL

★ Uni-directional level translation : 5V CMOS ⇒ 3.3V LVTTL

★ CBTD Products: 'CBTD3306, 'CBTD3384, 'CBTD16210, 'CBTD16211
- in SOIC, SSOP, TSSOP and **TVSOP Packages**

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If a device with the capability to switch bus signals on or off is needed, then TI's CBT bus switch can be used to support easy bus communication.

CBT devices serve a number of unique applications in PC, Workstation, Bus Board, Telecom, Industry and Hard Drive end-equipment markets.

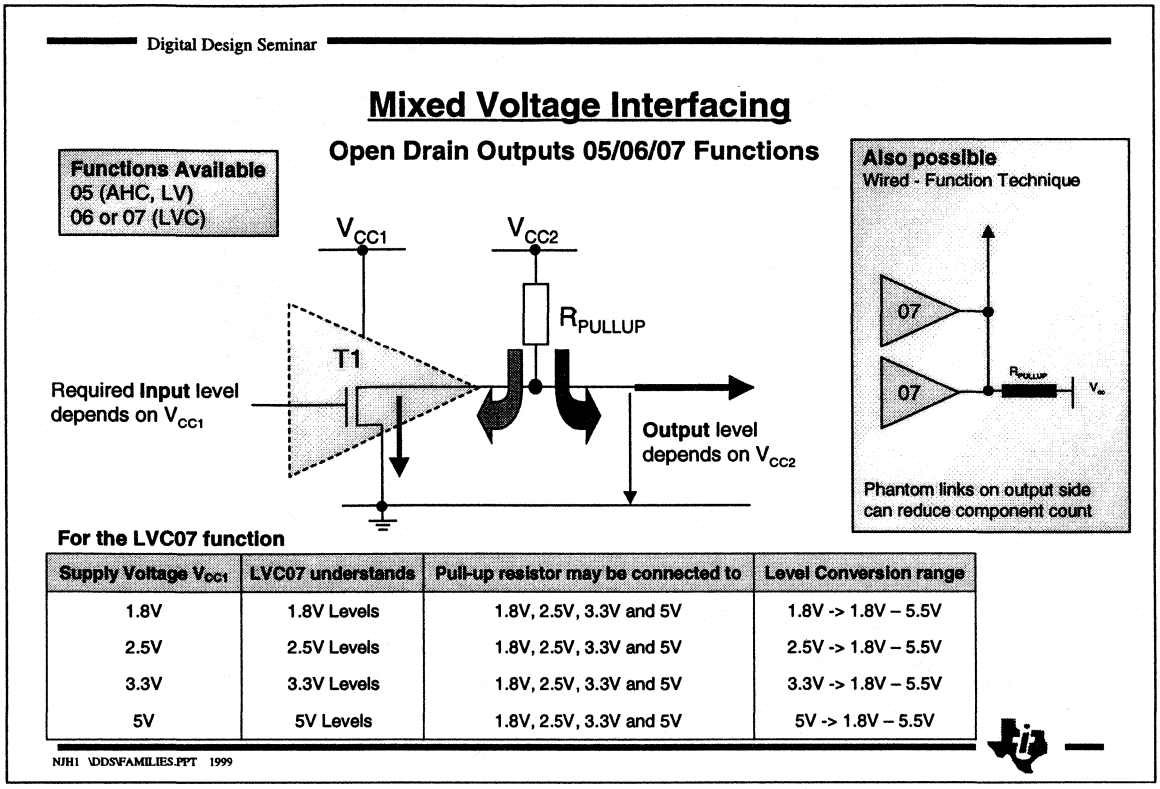
A CBT switch consists of simple n-channel MOS transistors. When the switch is open, it provides isolation (3-state) for the bus line. When the switch is closed, it imposes a near-zero propagation delay on the line (250 ps).

In multiprocessor systems, CBT can be used for extremely fast bus connections, bus exchanges in crossbar systems, memory interleaving, bus byte-swapping and a variety of other switching functions.

CBT switches also serve as **5-V to 3.3-V bus translators**, helping designers to mix devices of different voltage levels in the same system. Three different CBT bus switches with integrated diode (CBTD) are available from Texas Instruments.

Extremely low propagation delays of 250ps make CBT devices an effective replacement for drivers and receivers in high-speed systems, where signal buffering is not required.

In addition, **low power consumption** helps to improve battery life in portable systems. Small foot-print packages save board space.



The above foil shows two typical uses for open drain devices. Level shifting is possible since the pull-up resistor effectively connects the output of the device to any required V_{CC}, thus providing the necessary output switching voltage to an input. However, the maximum parameters of the device i.e. I/O voltages and current must not be exceeded.

Care must be also taken to choose the correct R_{PULLUP} value.

R_{PULLUP} calculated from the current requirements of the **inputs of the receivers**

R_{PULLUP} must be high enough to **limit the current into the conducting transistor T1**

The second benefit from open-drain devices is that extra logic functionality can be built into a system, without the need for additional gate devices. The example above shows how a active-LOW wired-OR / AND and an active-HIGH wired-AND can be implemented.

By using the following table, one can see that, depending if the logic is active-HIGH or active LOW, wired functions can be achieved.

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

If logic is active-HIGH, only time the output (Q) is high is when all inputs are high. This results in an AND function.

This kind of application is also useful, since a gate with n inputs can be implemented and no extra active components are needed.

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5 Volt ⟷ 3.3 Volt Interfacing Capability

from \ to	SN74ALVT	SN74LVT	SN74LVC	SN74ALVC	SN74AVC	SN74LV	5V CMOS (CMOS levels)	5V TTL HCT/ACT/AHCT
SN74ALVT	☑	☑	☑	☑	☑	☑	Use Level Shifters	☑
SN74LVT	☑	☑	☑	☑	☑	☑		☑
SN74LVC	☑	☑	☑	☑	☑	☑		☑
SN74AVC	☑	☑	☑	☑	☑	☑		☑
SN74ALVC	☑	☑	☑	☑	☑	☑		☑
SN74LV	☑	☑	☑	☑	☑	☑		☑ *
5V CMOS (HC/AC/AHC/..)	☑	☑	☑	Use input voltage divider	Use input voltage divider	☑	☑	☑ *
5V TTL (ALS/F/AS/..)	☑	☑	☑	☑	☑	☑	Use pull-up resistor to 5V	☑
ACT/HCT	☑	☑	☑	Use input voltage divider	Use input voltage divider	☑	☑	☑ *

* limited by output drive capability of HC(T) , AHC (T) , LV

The AVC Family maintains 3.3V Tolerance even when V_{CC} is 2.5V and 1.8V

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Four different signal level combinations may have to be addressed in mixed mode design:

5V TTL	→	*3.3V TTL*
3.3V TTL	→	*5V TTL*
5V CMOS	→	*3.3V TTL*
3.3V TTL	→	*5V CMOS*

While the first two are very easy to address, the last two are difficult, as a certain technology may not support their requirements. LV, LVC, LVT and ALVT have I/Os that are 5V CMOS tolerant. Interfacing a 3.3V part to a 5V system that expects CMOS levels, however, usually requires a dedicated level shifter. CMOS levels are specified as follows:

$$V_{IL} = 0.3 \times V_{CC}$$
$$V_{IH} = 0.7 \times V_{CC}$$

The driver should at least be able to deliver:

$$V_{OL} < 0.3 \times V_{CC}\text{min} = 1.35V \quad (\text{with } V_{CC}\text{min} = 4.5V)$$
$$V_{OH} > 0.7 \times V_{CC}\text{max} = 3.85V \quad (\text{with } V_{CC}\text{max} = 5.5V)$$

This also implies that a standard 3.3V output does not deliver a high enough output voltage to reliably drive 5V CMOS inputs.

Even with a pull-up resistor

$$V_O\text{max} = V_{CC}\text{min} + 0.7V \text{ (diode)} = 3.7V < 3.85V$$

The result is the following: A special **'Level-Shifter'** is required (see previous pages).

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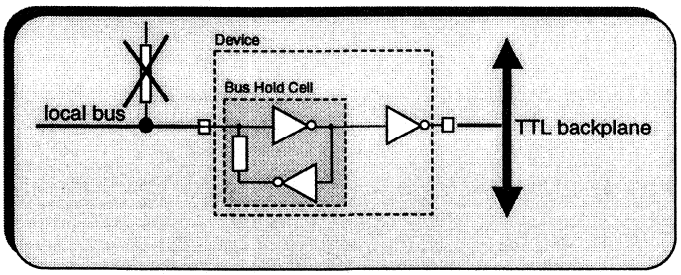
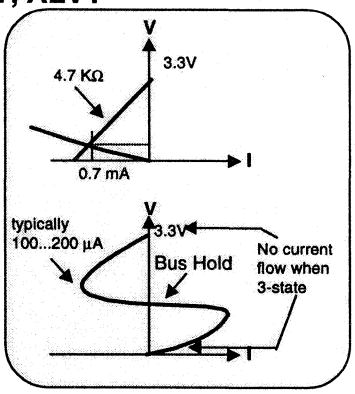
Bus Hold Input Characteristic

CBT, ABT, LVC, ALVC, AVC, LVT, ALVT





- Holds the last known state of the inputs
- Provides for +/- 74 µA of holding current at 0.8 and 2.0V
- Bus Hold current does **not** load the driving output at a valid logic level
- Negligible impact to input/output capacitance (0.5pF)
- Eliminates the need for external resistor on unused or floating I/O pins
- Reduces the number of passive components per board
- Implemented in ALVT, LVT,ALVC,selected CBT, LVC, AVC and ABT functions
  - Bus Hold nomenclature : SN74xxxHxxx; e.g. SN74LVCH245

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TI has addressed many important design issues including testability, memory driving, bus termination, low skew requirements, and low-impedance line driving with specialized, advanced logic devices that improve overall system performance.

This figure shows the typical V-I characteristics of a bus line with pull-up resistors versus a bus line using a bus interface device with integrated bus hold. The bus hold circuit basically consists of a non-inverting driver that will drive a small current (typically the peak value is about 100-200µA) back into the bus, to pull it back to proper signal levels, if the bus is floating.

As can be seen, the **pull-up solution causes a constant current to flow** at both ends. The **bus hold circuit**, on the other hand, not only consumes much less current, but also does not represent any static loading to the bus. This means that it will not consume any current, as long as the bus is at a proper LOW or HIGH level.

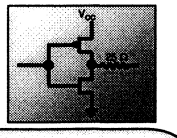
The Bus Hold feature has been implemented in the ALVT, LVT and ALVC family as well as in selected CBT, LVC, AVC and ABT functions.

Look for the '**H**' in the device nomenclature.

Digital Design Seminar

Series Termination - Devices

ABT, LVC, ALVC, LVT, ALVT



- Series Resistor at Output stage
- Short propagation delays & low power consumption
- Supports highest system performance and/or use of slower memories
- Reduces component count, board space, mounting costs

Function	Description	Family				Function	Description	Family		
		ABT	LVTH	ALVC	LVC			ABT	LVTH	ALVC
'2240	8- bit mem. drv.	✓				'162374	16-bit D-flip-flop		✓	✓ 1)
'2241	8- bit mem. drv.	✓				'R162409	9-bit, 4-port bus exchr.			✓
'2244	8- bit mem. drv.	✓			✓	'162460	4 to 1 bit mem. drv/mux.	✓		
'(R)2245	8- bit mem. drv.	✓	✓		✓	'162500	18-bit memory UBT ™	✓		✓ 1)
'2827	10 - bit mem.drv	✓				'162501	18-bit memory UBT ™	✓		✓ 1)
'5400	11- bit mem. drv.	✓				'162525	18-bit reg.bus trans.			✓
'5401	11- bit mem. drv.	✓				'162540	16-bit buffer drv.			✓ 1)
'5402A	12- bit mem. drv.	✓				'162541	16-bit buffer drv.		✓	✓ 1)
'5403	12- bit mem. drv.	✓				'162601	18-bit memory UBT ™	✓	✓ 1)	✓
'162240	16-bit mem. drv.		✓			'162721	20-bit D-ff,clk enable			✓
'162241	16- bit mem. drv.		✓			'162820	10-bit FF w dual Output	✓		✓
'162244	16- bit mem. drv.	✓	✓	✓	✓	'162823	18-bit Bus Interf. FF	✓		
'(R)162245	16- bit mem. drv.	✓	✓	✓	✓	'162825	18-bit mem.drv	✓		
'162260	12 to 24-bit mem.drv/mux.	✓		✓		'162827	20-bit mem. drv.	✓		✓
'162268	12 to 24-bit reg.bus exchr.			✓		'162830	1-2 addr.drv.			✓
'R162269	12 to 24-bit reg.bus exchr.			✓		'162831	1-4 addr. drv.			✓
'162334	16-bit universal bus driver			✓		'162835	18- bit univers. bus drv.		✓ 1)	✓
'162344	8-bit 1:4 addr line drv.			✓		'162836	20 bit univers. Bus drv.			✓
'162373	16-bit transp. latch		✓	✓ 1)		'162841	20-bit D-latch			✓

As of September '98

1) planned

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One line termination technique, which was already discussed in the 'Basics and Practical Examples of Transmission' is the so-called **Series Termination.**

As opposed to most other termination techniques (where the lines are terminated at the end), here the **driver output impedance is matched with the line impedance by adding a series resistor**. This means that no reflection will occur on the driver side.

It is thus a very efficient method for a point-to-point connection, or for a line driving a concentrated load. This technique is especially useful when driving memory array address lines as it suppresses signal under- and overshoots which may otherwise lead to data loss.

Several 5-V and 3.3-V logic devices are available with an integrated output resistor. The resistor value is typically around 25Ω, leading to an effective output resistance of about 33Ω.

As a certain impedance mismatch is acceptable, these circuits will be feasible for an line impedance up to approximately 75Ω.

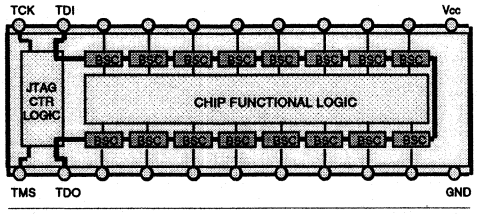
TI's new **AVC** family eliminates the need for damping resistors though the **DOC™** circuit. This circuit automatically lowers the output impedance during switching and then increases it after the threshold voltage has been reached to avoid over- and undershoot normally associated with fast switching logic devices.

Digital Design Seminar

Texas Instruments IEEE 1149.1 (JTAG) Products

Boundary scan products allow easy test of high-density boards

- ✶ SCOPE™ bus drivers support most applications demanding boundary scan functions
- ✶ Path support functions allow easy handling of scan path's in large systems



IEEE1149.1 was developed by the Joint Test Action Group (JTAG)

SCOPE (System Controllability Oberservability Partitioning Environment) is a trademark of Texas Instruments Incorporated

Benefits using IEEE1149.1

- ✶ Test node access on high-density board
- ✶ Inexpensive test adapters
- ✶ Std interface for ICs, boards, systems
- ✶ Easy to implement in ASICs
- ✶ Broad spectrum of bus driver functions
- ✶ 3.3-volt drivers already on the market
- ✶ Support from IC and ATE vendors

Product features

- ✶ State-of-the-art techniques used
- ✶ Popular bus driver functions available
- ✶ 5-V and 3.3-volt versions available
- ✶ Universal-Bus-Transceivers available
- ✶ Functions available for large systems

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ScopeTM products from Texas Instruments comply with the IEEE1149.1 specification.

Scope products are offered in BICMOS technology (ABT and LVT) and Advanced CMOS (ACT).

The nomenclature includes an '8' to express its testability feature (e.g SN74ABT8245, which is a '245 function additionally supporting testability (IEEE1149.1).

The Widebus devices including this feature can be recognized with '18' instead of '16' (e.g SN74LVT18502).

The generic IEEE1149.1 function:

Between each IC pin (input and output) and the chip functional logic there is a boundary scan cell (BSC).

All BSCs are connected to a serial scan path with the function of a shift register.

The BSCs are to be controlled via 4 control pins:

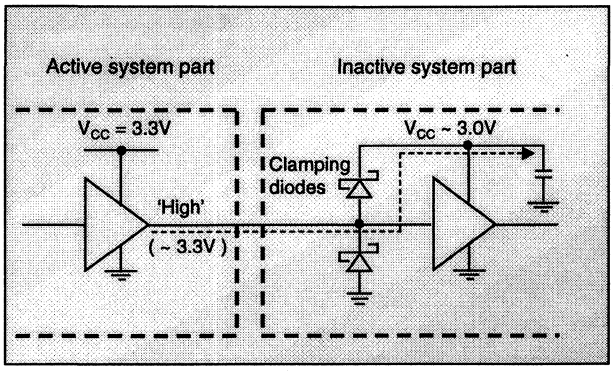
- TCK (test clock)
- TMS (test mode select)
- TDI (test data input)
- TDO (test data output).

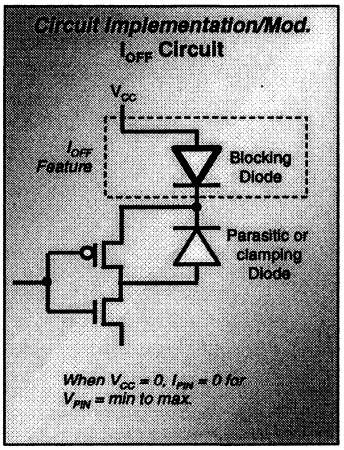
The BSC allows capturing data from and providing data to the chip data path.

Digital Design Seminar

Potential Problems in Partial Power Down Applications

* Unexpected device behaviour during power up or power down may cause malfunction
* Input signals start sourcing current through input clamping diodes





Logic Family I_{OFF} Specification	
ABT, LVT, ALVT	: ±100 µA
LVC, AVC	: ± 10 µA
LV	: ± 5 µA

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Along with the power reduction trend that drove the transition to 3.3V, live insertion has become of much more interest in system design. Also, so-called "**partial power down**" is being applied more frequently, where the supply voltage V_{CC} will be switched off in certain parts of the system, while these are not in use.

In both cases (live insertion and partial power down), there are two potential problems that need to be addressed. First, there is a risk of **unexpected device behaviour** during the power transition. All logic circuits available in the market have specifications that guarantee proper circuit operation only within a certain V_{CC} range. During power up or power down, the **circuit will be operated outside this range, which may lead to an unpredictable device response**. For example, the output may start sinking large currents or, worst case, even start oscillating.

Second, the block diagram shows a configuration, where an active device output is connected to a device, whose V_{CC} has been switched off. In this special case, the inactive circuit uses protection diodes as its inputs. This method is being used in many CMOS circuits for ESD protection. Unfortunately, a high signal applied to this input will be fed to the circuit's V_{CC} connection via the protection diode. **The V_{CC} level of the inactive circuit will be about 3.0V, which is high enough to activate this circuit and (via the V_{CC} path) the remaining devices in the inactive system part**. This may result in all kinds of unexpected system behaviour.

Consequently for ABT, LVC, LV, AVC, LVT and ALVT, TI has designed blocking diodes into the output stage V_{CC} path and has removed the input clamping diode up to V_{CC}. All families that have this characteristic have I_{OFF} specified in the datasheet.

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Live Insertion Support Aspects of Logic Families

	HC/ HCT	AC/ ACT	ALS/ F/AS	AHC/ AHCT	ABT	LV	LVC	ALVC	AVC	LVT	ALVT
Diode connects Inputs to V_{CC} if V_{CC}=0V	✗	✗	-	-	-	-	-	✗	-	-	-
Diode connects Outputs to V_{CC} if V_{CC}=0V	✗	✗	-	✗	-	-	-	✗	-	-	-
V_{CC} above which the circuit will typically work*	1.5V	2V	3.5V	1.5V	2.1V	1.5V	1.2V	1.2V	1.5V	1.5V	1.2V
Outputs will be tri-stated below this limit					✓					✓	✓

* Circuit will be functional but may still be outside AC specifications

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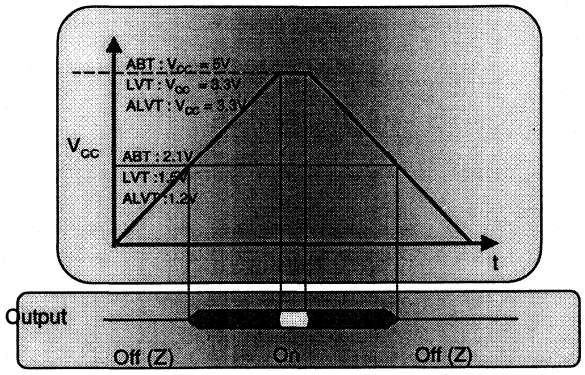
This table illustrates the feasibility of using certain logic families for live insertion applications.

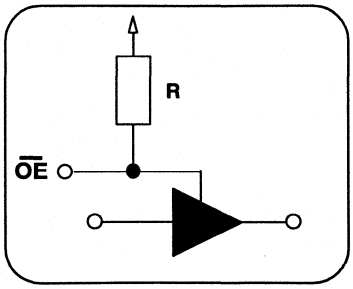
As can be seen, the 5V families HC/HCT and AC/ACT will be difficult to use in any power-down applications. This is mainly because they all use protection diodes that connect the inputs and outputs to V_{CC}.

Those families that do not use protection diodes to V_{CC} will be easier to design with. However, only **5V ABT, 3.3V LVT and 3.3V ALVT circuits feature full hot insertion** support, as they also contain a "power-up 3-state" circuitry that will 3-state the device outputs, if V_{CC} is below a certain limit. A system designer can thus easily design interfaces that allow reliable power-down operation.

Digital Design Seminar

Power Up 3-State Function
ABT, LVT, ALVT





tie external resistor from OE line to V_{CC}

* OE follows V_{CC}, ensuring device remains in 3-state (Z) during power-up/ down
  - See $I_{OZ(PU/PD)}$ on datasheet
* Devices tested at ramp rates of 200 µs/V -20 µs/V
* Another option: Use ABTE which has internal pull-up resistor

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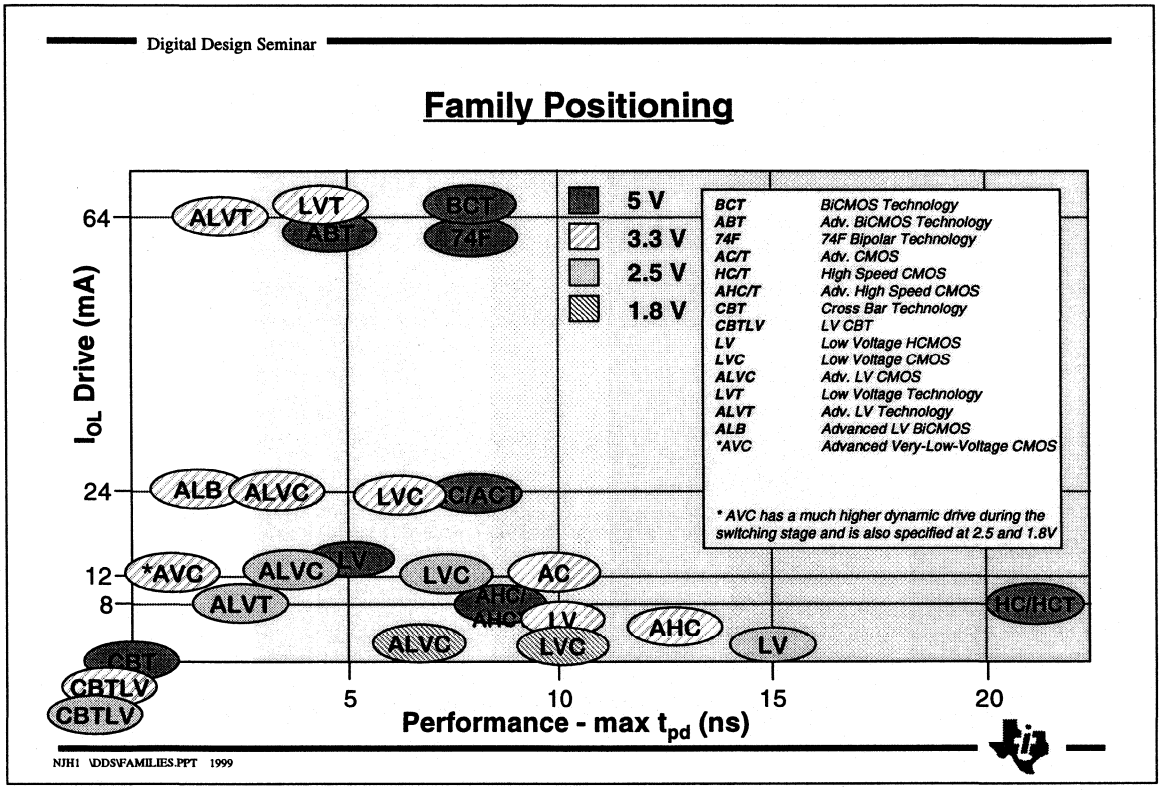
Power up 3-state is a favourite feature of designers that develop boards for hot insertion.

ABT, LVT and ALVT devices with this feature automatically ensure outputs are disabled during power up. Most other device families require a pullup resistor on the output enable to ensure valid outputs during power up.

In the datasheets, one can recognize the Power-Up 3-state functionality by the statement 'High-Impedance State during Power Up and Power down'. The parameters I_{OZPU}, I_{OZPD} define the Off-state output current, flowing into an output having 3-state capability.

For hot insertion and power-down applications the I_{OFF} specification is of importance as well. This is the amount of current that will flow into a circuit node when the device is powered down (V_{CC} = 0 V).



The above graph is usually the best way to compare all new logic families quickly.

The X-axis represents speed [ns] with the faster parts to the left.

The Y-axis represents output drive [mA] with higher drive towards the top.

The various colours indicate at which voltage node the respective families are specified.

As a general statement, all logic parts perform the same function if the "number" is the same. (e.g. ABT245, LVT245, AHC245, HC245 - all 8-bit transceivers with identical pinouts)

The AHC family fills the gap which existed for low drive but high speed devices in the 5V logic area. The only family fulfilling the requirements of low drive and compatibility to TTL and CMOS logic was the HC(T) family. The disadvantage of this family was its low speed.

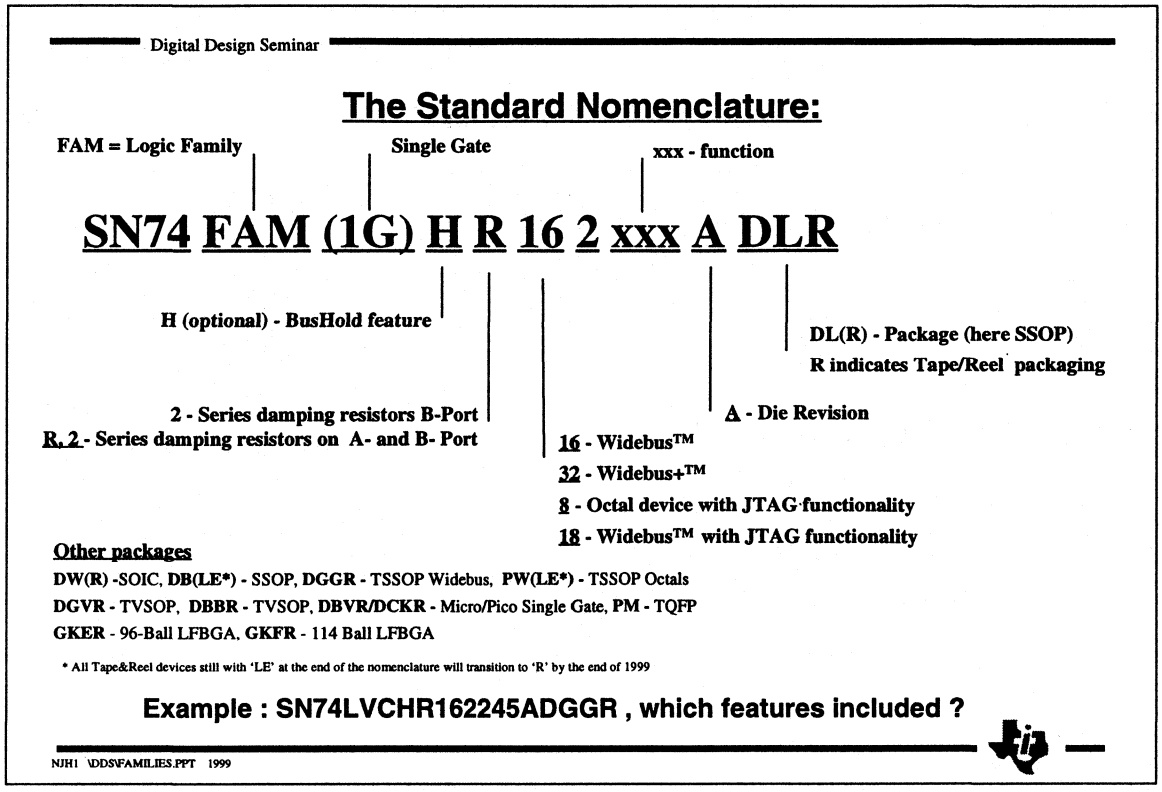
With the AHC(T) family TI closes this gap. Under 5V operation the speed of AHC(T) is comparable with the AC(T),74F,BCT family and has the low drive of HCMOS.

Furthermore, in some applications (considering the very low drive of I_{OH}, I = 4mA) AHC could also be operated under 3.3V.

Note that CBT and CBTLV bus switches have no drive and near zero propagation delay. This is because this family acts like a closed wire, unless being used for voltage translation.

Also shown on this foil are all our low-voltage families with their associated speed and drive performance at the different voltage nodes at which they are specified. As can be seen, almost all performance nodes are covered by our logic portfolio making Texas Instruments the complete logic solution supplier

AVC, the newest member of our Logic Portfolio, has both a static and dynamic drive since the output impedance is decreased during the switching phase by the DOC™ circuit.



This foil describes the standard Texas Instruments Logic (SN74) nomenclature.

Firstly, Texas Instruments has kept a policy of making things very simple when it comes to name logic families. TI always shows which family technology the device has been designed in :

After the SN74 prefix, the family technology will follow ie :

- LVC
- ALVT
- AHCT (AHC with TTL compatible inputs) etc...

Secondly, TI provides an easy way to recognise which features are included in a particular logic device:

- **H** for Bus**H**old
- **R** for Series **R**esistors

And finally, Texas Instruments maintains a consistent and easy to follow package naming strategy. As one can see above, each difference package has a unique identifier code, which is ended by an '**R**' if the device is sold on a **R**eel.

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Logic Families Summary

High Speed
- Critical Points : Slew rate and propagation delay

High Drive
- Incident Wave Switching

Low Power
- Move to lower voltage families

Ease of Use
- Bushold, 5V Tolerance, I_{OFF}, Hot-insertion

Advanced Packaging
- Smaller packages - Less board space
- Lower lead inductance - Better performance

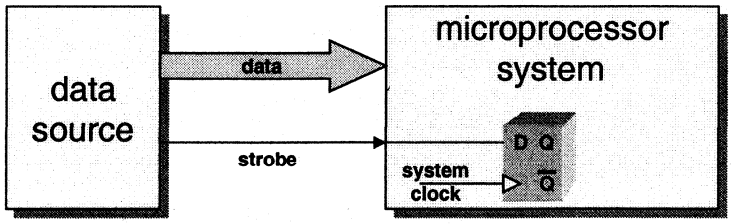
Digital Design Seminar

Agenda

- ★ Introduction
- ★ Basics and Practical Examples of Transmission
- ★ Logic Families
- ➢ Metastability
- ★ System Design Criteria
- ★ Bus Systems
- ★ Advanced Logic Trends

Digital Design Seminar

The Synchronization Problem



- ★ **Microprocessors are synchronous systems.**
- ★ **Data sources (peripheral devices, memories, etc.) provide data mostly asynchronously with respect to the microprocessor.**
- ★ **Therefore the control signals of the data source have to be synchronized to the system clock.**
- ★ **In synchronization circuits the timing requirements of flip-flops (t_{su}, t_h) are violated.**

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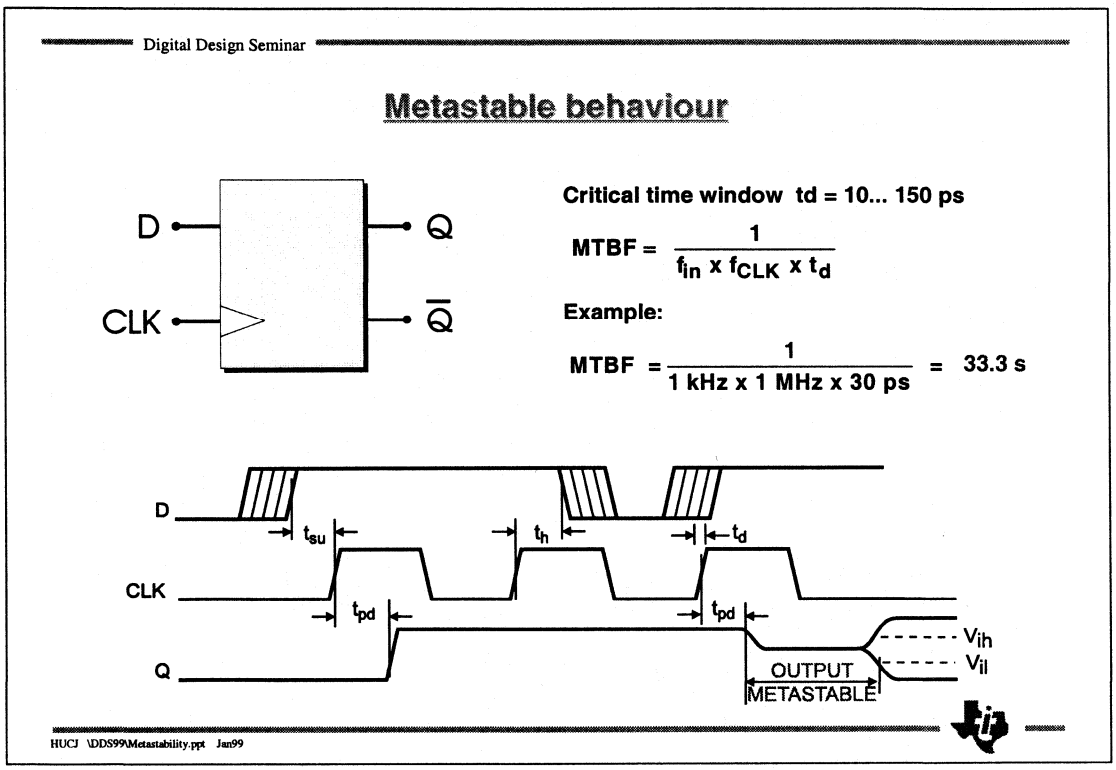
Standard microprocessor systems are synchronous systems, which means that there is a common clock signal that feeds the clock inputs of all flip-flops in the system. Under these circumstances it's easy to fulfill the set-up and hold-time requirements of all flip-flops.

It's a common situation that external data has to be transferred into a microprocessor system; and generally the external equipment runs asynchronously to the clock of the microprocessor system. In this situation it's usual to put the new data word onto the data lines and use a separate strobe line to indicate the presence of the new data. Anywhere within the microprocessor this strobe signal will be stored in a flip-flop, whose clock is synchronous to the microprocessor clock.

Under these circumstances the designer cannot ensure that the set-up or hold-time requirements of this flip-flop will be fulfilled. If a violation of the set-up or hold-time takes place, the manufacturer of the flip-flop will no longer guarantee proper function and the system may malfunction.



Every flip-flop data-sheet specifies a set-up and a hold time. The set-up and hold-time define a time window around the active (mostly rising) edge of the clock signal, where it is not allowed to change the signal at the D-input. If the signal at the D-input changes within the forbidden set-up and hold-time window, one of two reactions of the flip-flop can be observed:

1) The flip-flop works perfectly with no special behaviour

2) The output of the flip-flop becomes metastable

If the output of a flip-flop is metastable, the voltage value V_O is higher than the V_{il} low-level-limit, but lower than the high-level-limit V_{ih}: It is in the forbidden area between low and high. This situation can last less than 1ns, but could also last longer than 30ns. This normally is a major problem for the input of the circuit that gets its signal from this metastable flip-flop.

Because it's not possible to avoid this situation by design, the only way to deal with it is statistically. The value used here is MTBF (**M**eantime **b**etween **f**ailure) and can be calculated using the following formula:

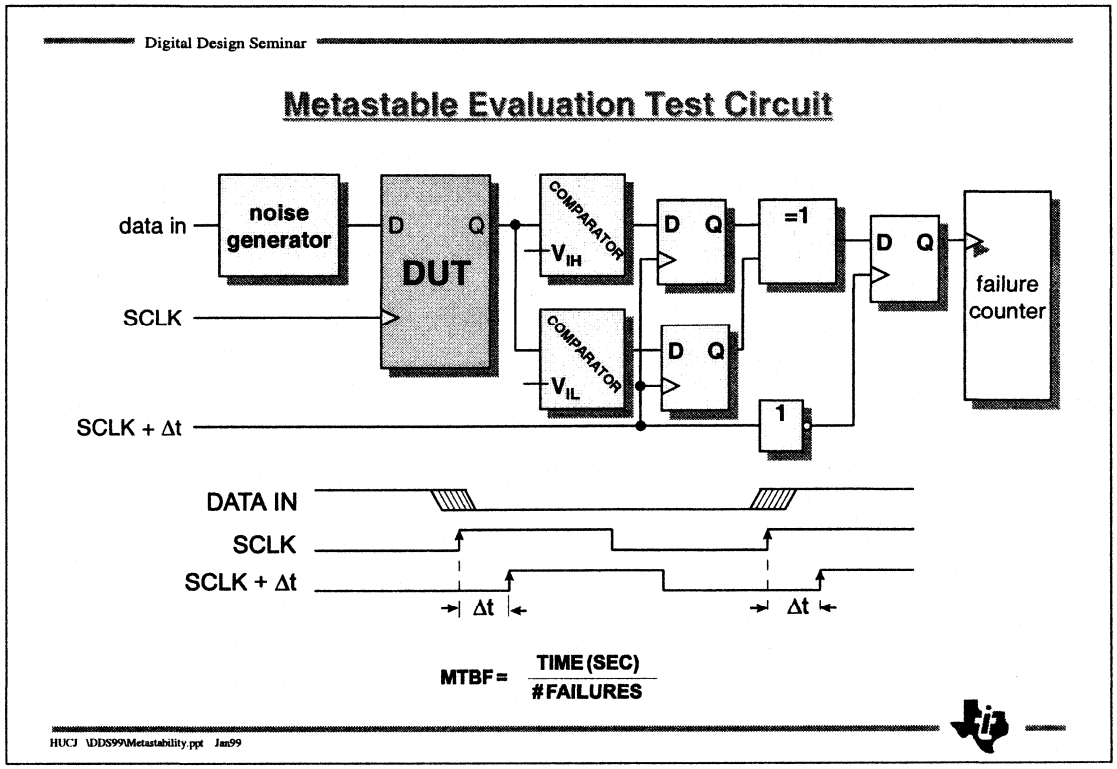
$$MTBF = \frac{1}{f_{in} \times f_{CLK} \times t_d}$$

with f_{in}: Data rate at D-input

f_{CLK}: Clock frequency

t_d: Critical time window

The set-up and hold-time window is a time window guaranteed by the manufacturer of the flip-flop, guaranteed over the temperature range, supply voltage range and production variations. If the signal at the D-input changes within the critical time windows t_d, then the flip-flop will become metastable. The above example with MTBF = 33.3s shows a unacceptable situation.

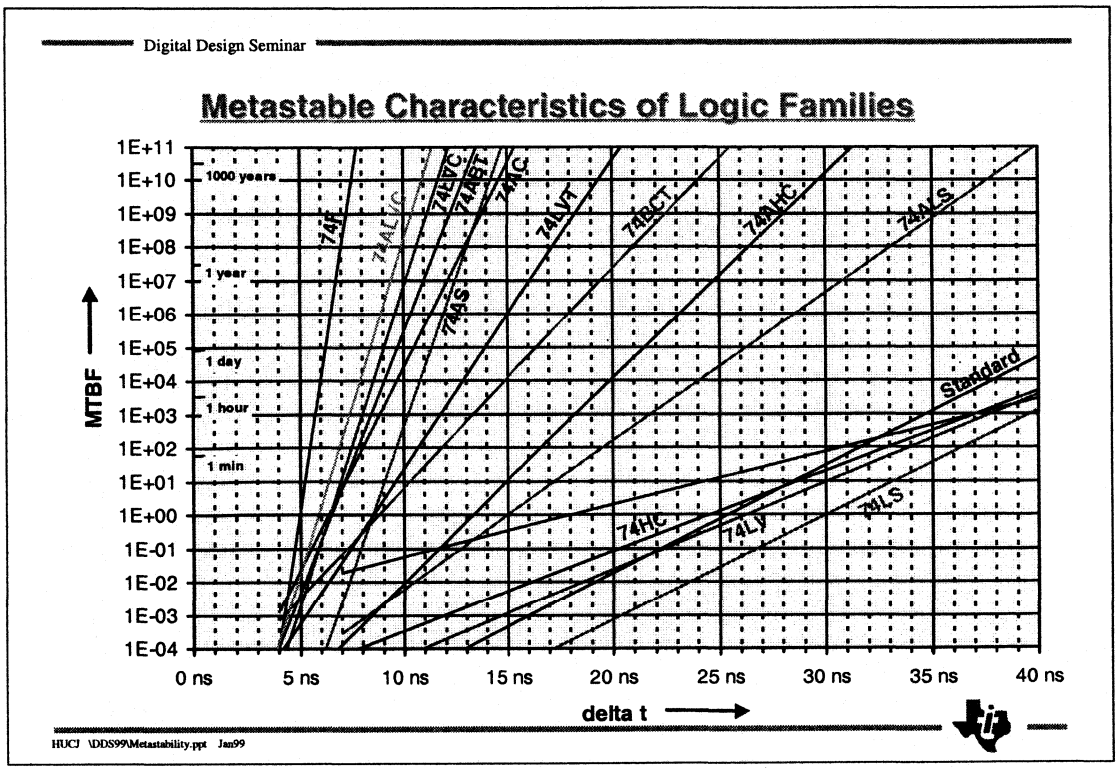


To find out the metastable behaviour of the flip-flops from Texas Instruments, the applications lab has made measurements with the above setup:

The flip-flop under test (DUT) gets a stable clock signal and a data signal with some jitter. The output of the flip-flop is connected to two comparators, one for the comparison against a valid logic high level V_{ih} and one for the valid logic low level V_{il}. The result of this comparison is stored in two flip-flops, whose clock signal is the delayed clock of the tested flip-flop (DUT). The following EXOR gate filters the errors and sends them to a ordinary counter.

With the amount of delay that is added to the clock signal of the two comparators flip-flops, we give some time to the tested flip-flop to make the decision between a logic high- and low-level. If the flip-flop wasn't able to make this decision within the specified time-frame, and the output of the flip-flop is still within the forbidden voltage area, a metastable state will be counted with the failure counter.

Some of these tests have to be running over several days to find a reasonable number of metastable conditions.



The Applications Lab of Texas Instruments measured the flip-flop of all available product families with the test set-up described one page before. The result of these measurements can be seen in the above diagram.

In X-direction the diagram shows Δt, the time-frame the flip-flop gets to make a decision for high or low, and the Y-axis applies to the resulting meantime between failure (MTBF) rate.

These curves have been measured with a clock frequency of 1MHz and an input data rate of 500 kHz.

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Mean Time between Failures of a Synchronizer

$$MTBF = \frac{e^{(T \times \Delta t)}}{f_{in} \times f_{CLK} \times T_0}$$

- ★ There is no way to avoid metastable states in synchronization circuits.
- ★ Fast Logic Circuits return quicker from a metastable to a stable state.
- ★ The probability of system failures is greatly reduced by a delayed test of the synchronization circuit.

	T	T_0
74STD	0.74 ns^{-1}	2.9 x 10^{-4} s
74LS	0.72 ns^{-1}	4.8 x 10^{-3} s
74S	0.36 ns^{-1}	1.3 x 10^{-9} s
74ALS	1.02 ns^{-1}	8.8 x 10^{-6} s
74AS	4.03 ns^{-1}	1.4 x 10^{3} s
74F	9.20 ns^{-1}	1.9 x 10^{8} s
74BCT	1.51 ns^{-1}	1.14 x 10^{-6} s
74ABT	3.61 ns^{-1}	0.033 s
74HC	0.55 ns^{-1}	1.48 x 10^{-6} s
74AHC	1.41 ns^{-1}	2.9 x 10^{-4} s
74AC	2.80 ns^{-1}	1.1 x 10^{-4} s
74LV	0.60 ns^{-1}	1.38 x 10^{-5} s
74LVC	4.40 ns^{-1}	4.008 s
74ALVC	4.60 ns^{-1}	1.047 s
74LVT	2.13 ns^{-1}	1.52 x 10^{-4} s

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The following equation is the mathematical representation of the graphs on the previous page:

$$MTBF = \frac{e^{(T \times \Delta t)}}{f_{in} \times f_{CLK} \times T_0}$$

with f_{in}: Data rate at D-input

f_{CLK}: Clock frequency

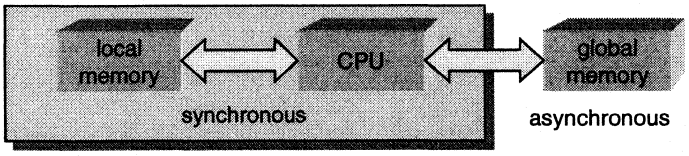
T and T_0: Constants describing the device family characteristics

Δt: time for the flip-flop to decide between high or low

With this equation it's possible to calculate the MTBF rate of a specific circuit design.

Digital Design Seminar

Calculation of System Reliability



Assumptions: System clock rate: 33 MHz

Average access rate to the global memory: 100 kHz

Logic family: SN74LVT

Required: Mean time between failure: > 100 years

$$\textbf{100 years} = 3.2 \times 10^{9}\,\text{s} = \frac{e^{(2.13\,\text{ns}^{-1} \times \Delta t)}}{100\,\text{kHz} \times 33\,\text{Mhz} \times 1.52 \times 10^{-4}\,\text{s}}$$

$$\Delta t = 20\ \text{ns}$$

To meet the required system reliability, the test of the synchronization circuit output signal has to be delayed by 20 ns.

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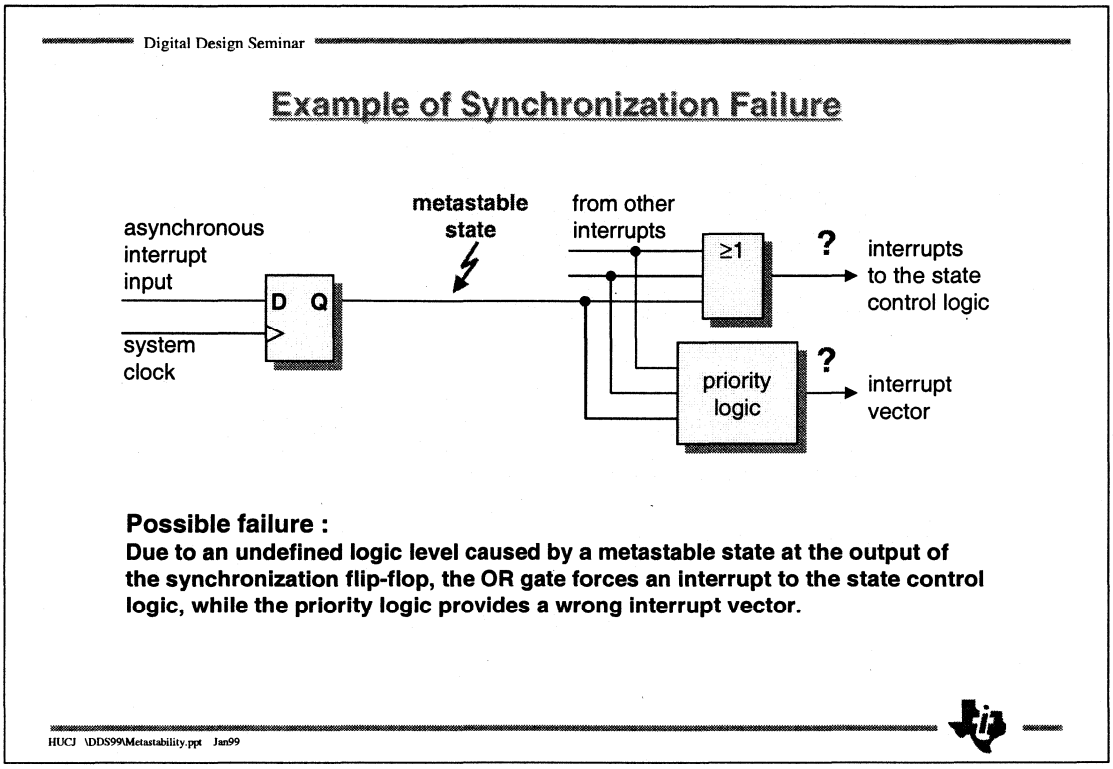
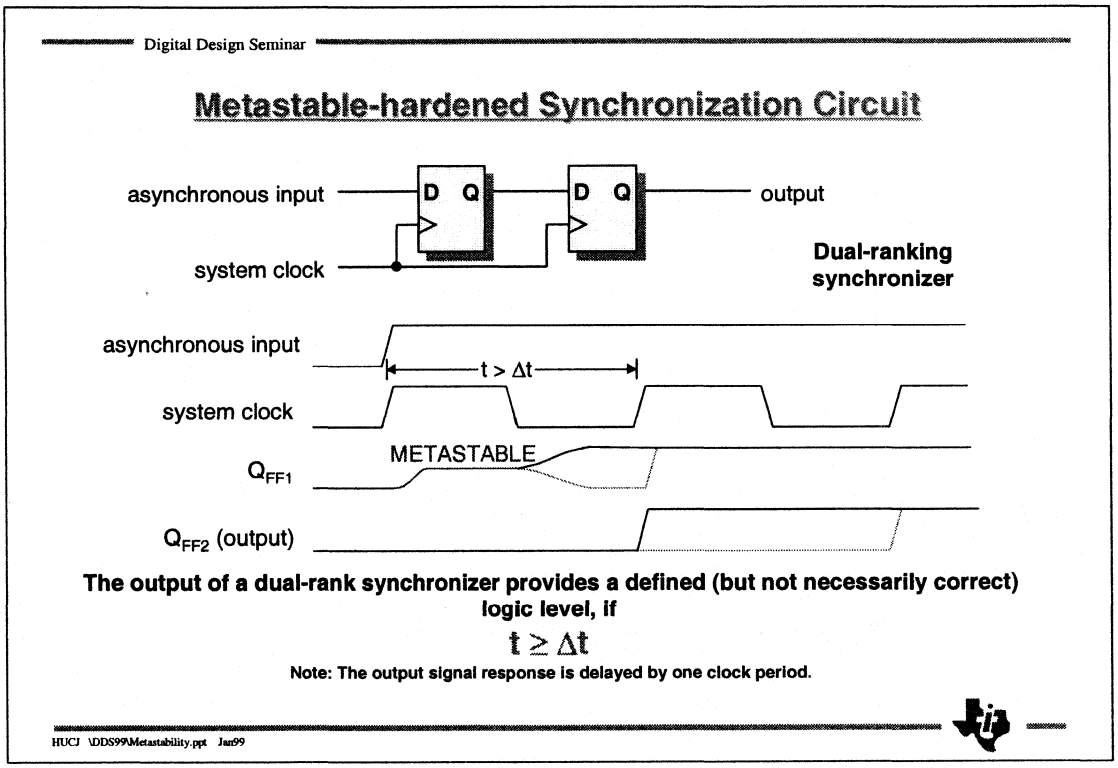
In the above example a CPU, running with 33MHz clock frequency, accesses a external global memory with an average data rate of 100kHz. The designer wants to use a SN74LVT flip-flop and needs a meantime between failure rate of 100 years. Using the equation of the page before, Δt can be calculated to be 20 ns. This means, that if the CPU waits 20ns after the active clock edge before it looks at the output of the SN74LVT flip-flop, an MTBF rate of 100 years is achieved.



In the first example (page 3-2) the metastable states could be supervised by intelligent software: The CPU looks at the STROBE signal twice before it accepts the logic state.

The example above shows a situation where metastability must be solved by hardware. Assume the output of the interrupt flip-flop is metastable and correspondingly the logic level is undefined. The gate that sends the interrupt to the CPU can detect a valid interrupt while the priority logic takes the same signal and decides that there is actually no interrupt. Therefore an interrupt occurs, but no interrupt (or a wrong) vector is sent to the CPU. In this case the CPU possibly will jump to a not existing interrupt service routine and a system crash will be the result.



To increase the MTBF rate a further circuit design method is available: The **Dual-Rank Synchronizer**. Here we take two flip-flops and connect them as a shift-register. In this case the output of the second flip-flop will be less often in a metastable condition than the output of the first flip-flop. Three situations can occur when flip-flop 1 is in metastable state:

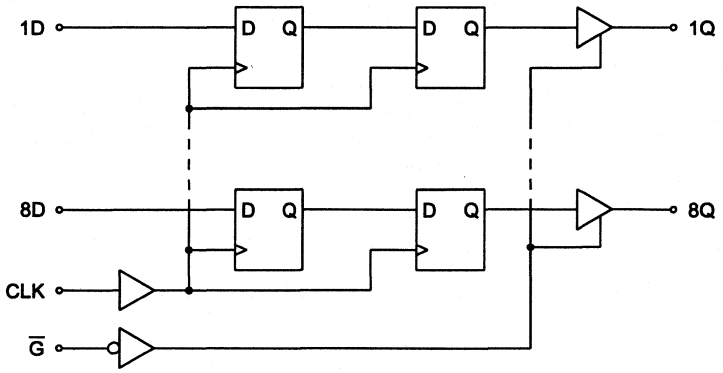
1) The metastable state of the first flip-flop is short enough, so at the next rising edge of the clock signal the second flip-flop already gets a good signal at its D-input.
2) The metastable state of the first flip-flop lasts longer than one clock period, but the second flip-flop accepts the undefined signal as a valid high or low state.
3) The metastable state of the first flip-flop lasts longer than one clock period and the second flip-flop becomes metastable, too.

In the first two cases the output of the second flip-flop is not metastable, while the first one is metastable. This shows the reduction of metastable states with this circuit.

Digital Design Seminar

Circuits for Synchronizer Applications

Improved system reliability due to dual-rank synchronizer SN74AS4374



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Because dual-rank synchronizers are a common way to reduce the occurrence of metastable states, Texas Instruments invented the SN74AS4374. This circuit has nearly the same function as the well known octal flip-flop SN74AS374, with the only difference that there is a dual-rank synchronizer instead of a single flip-flop in each data-path. Here no extra board space and no redesign is necessary to upgrade a single flip-flop synchronizer to a dual-rank synchronizer.

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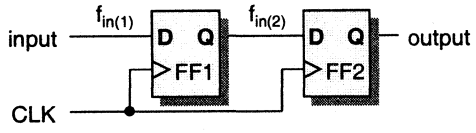
Mean Time between Failure of a Dual-rank Synchronizer

$$MTBF(2) = \frac{e^{(T \times \Delta t)}}{f_{in(2)} \times f_{CLK} \times T_0}$$



$$f_{in(2)} = \frac{1}{MTBF(1)}$$

$$= \frac{f_{in(1)} \times f_{CLK} \times T_0}{e^{(T \times 1/f_{CLK})}}$$

$$MTBF(2) = \frac{e^{(T \times t)} \times e^{(T \times 1/f_{CLK})}}{f_{in(1)} \times f_{CLK}^2 \times T_0^2}$$

Note: The flip-flop (2) will only fall into a metastable state, if the output of flip-flop (1) violates the timing requirements at the input of flip-flop (2)

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To calculate the MTBF rate of a dual rank synchronizer only the metastability of the second flip-flop is of interest. Here we use the formula previously discussed:

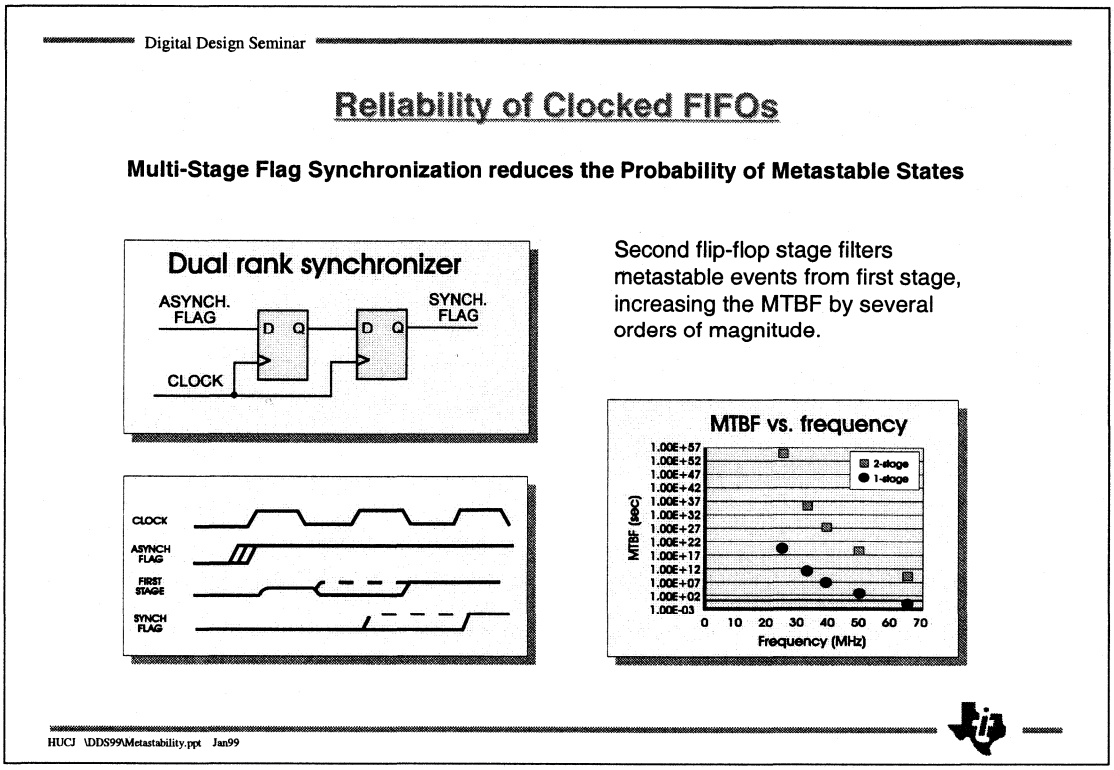
$$MTBF = \frac{e^{(T \times \Delta t)}}{f_{in} \times f_{CLK} \times T_0}$$

It's not possible to generate a metastable state at the output of the second flip-flop if the first flip-flop is working well. To drive the second flip-flop into metastable condition a metastable state of the first flip-flop is necessary. Hence the input data of flip-flop two that is of interest regarding metastability is only the situation where the first flip-flop is metastable. So the reciprocal MTBF value of the first flip-flop can be used as input data rate of the second flip-flop.

$$f_{in(2)} = \frac{1}{MTBF(1)} = \frac{f_{in(1)} \times f_{CLK} \times T_0}{e^{(T \times 1/f_{CLK})}}$$

Now the final formula can be calculated:

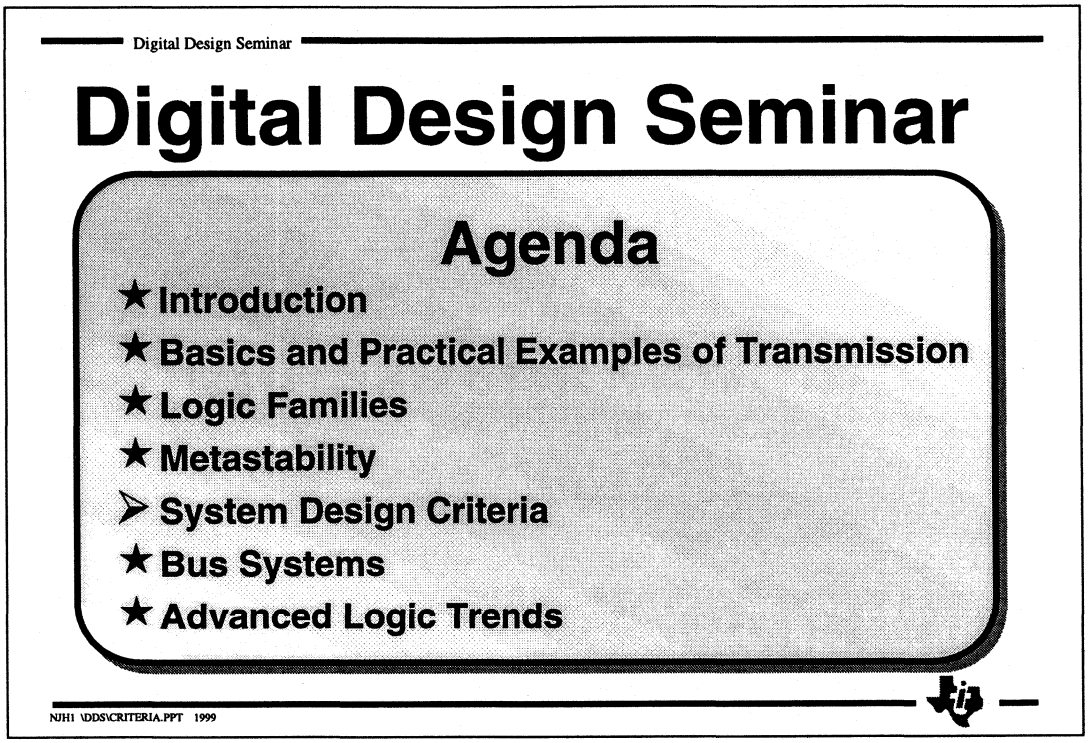
$$MTBF(2) = \frac{e^{(T \times t)} \times e^{(T \times 1/f_{CLK})}}{f_{in(1)} \times f_{CLK}^2 \times T_0^2}$$



Texas Instruments offers FIFO (first-in-first-out) memories. One key feature here is the possibility of asynchronous write and read operations. This is a product where metastability is a major issue and Texas Instruments uses at least dual-rank synchronizers to avoid metastable conditions at the outputs.

During the design phase investigations took place to find out the MTBF rate of FIFOs with and without dual-rank synchronizers. The result of these investigations can be seen in above diagram. For example at a clock frequency of 50 MHz the single flip-flop synchronizer shows a MTBF rate in the range of several minutes, while the dual-rank synchronizer is in the range of 10^{19} seconds or 3.17×10^{11} years.

This example shows the tremendous improvement this type of circuit design can achieve regarding metastable behavior.


Digital Design Seminar
Digital Design Seminar
Agenda
★ Introduction
★ Basics and Practical Examples of Transmission
★ Logic Families
★ Metastability
➢ System Design Criteria
★ Bus Systems
★ Advanced Logic Trends
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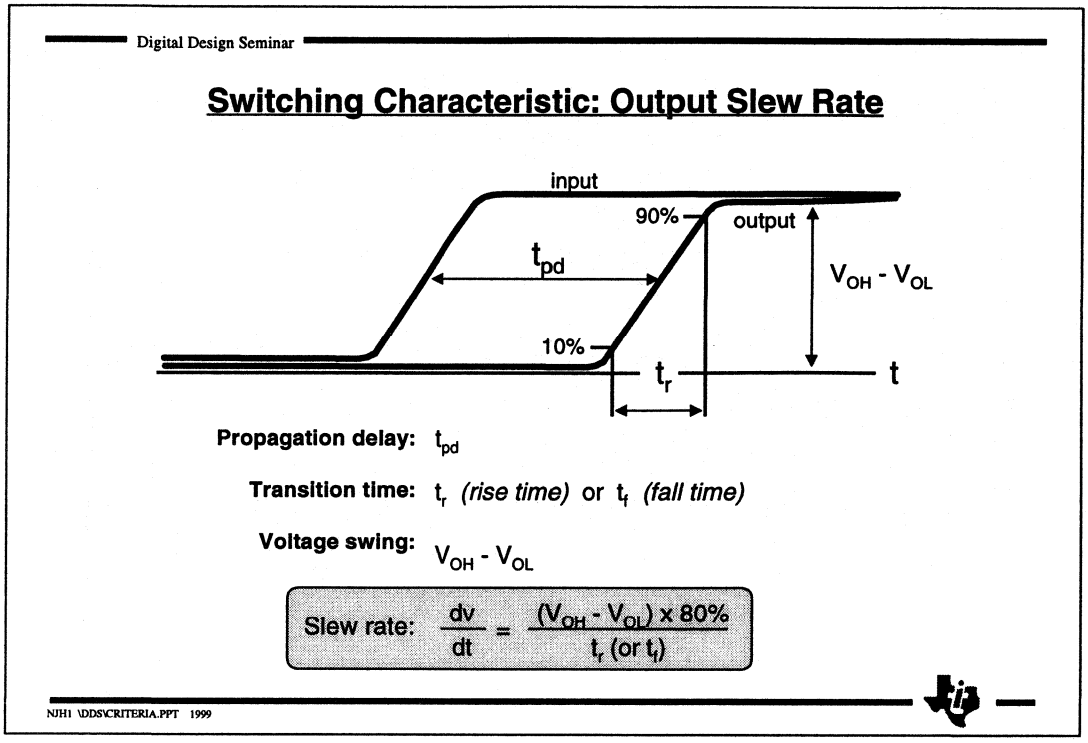

Noise in digital logic systems can arise from different sources:

- External noise radiated into the system
- Power-line noise coupled through the AC and DC power distribution system
- Crosstalk induced into signal lines from adjacent signal lines
- Signal- and supply-current spikes caused by switching several loads
- Transmission-line reflections through unterminated transmission lines.

The integrated circuits themselves are the major source of noise, simply because of the high-speed switching characteristics associated with these devices.

It can be seen from the formula above, that a circuit's slew rate corresponds to the transition (rise or fall) time of the output signal. The shorter the rise or fall time, the higher the slew rate.

Knowing the slew rate is good to get a rough idea on the potential noise that a logic device can cause. However, keep in mind that propagation delay and slew rate are not necessarily proportional.

Digital Design Seminar

Switching Characteristic
Slew Rate - 5-V and 3.3-V Logic

	F	ALS	ABT	AC	HC	AHC	AHC	LV	LVC	ALVC	LVT	ALVT	AVC
Propagation delay (ns)	3.6	6	2.9	4.1	9.9	4.0	5.3	8.0	4.1	2.1	2.4	1.5	1.2
Voltage Swing (V)	3	3	3	4.8	4.8	4.8	3	3	3	3	3	3	3
Slew Rate (V/ns)	1.3	1.0	1.0	1.8	0.9	0.8	0.5	0.7	0.9	1.3	1.2	1.4	1.0
	V_{CC} = 5 V						V_{CC} = 3.3 V						

- Example: '244 function ('16244 in case of ALVC), outputs loaded with 500 Ω, 50 pF; all values are typical
- Slew rate values shown are the higher ones of rising and falling edge of output signal

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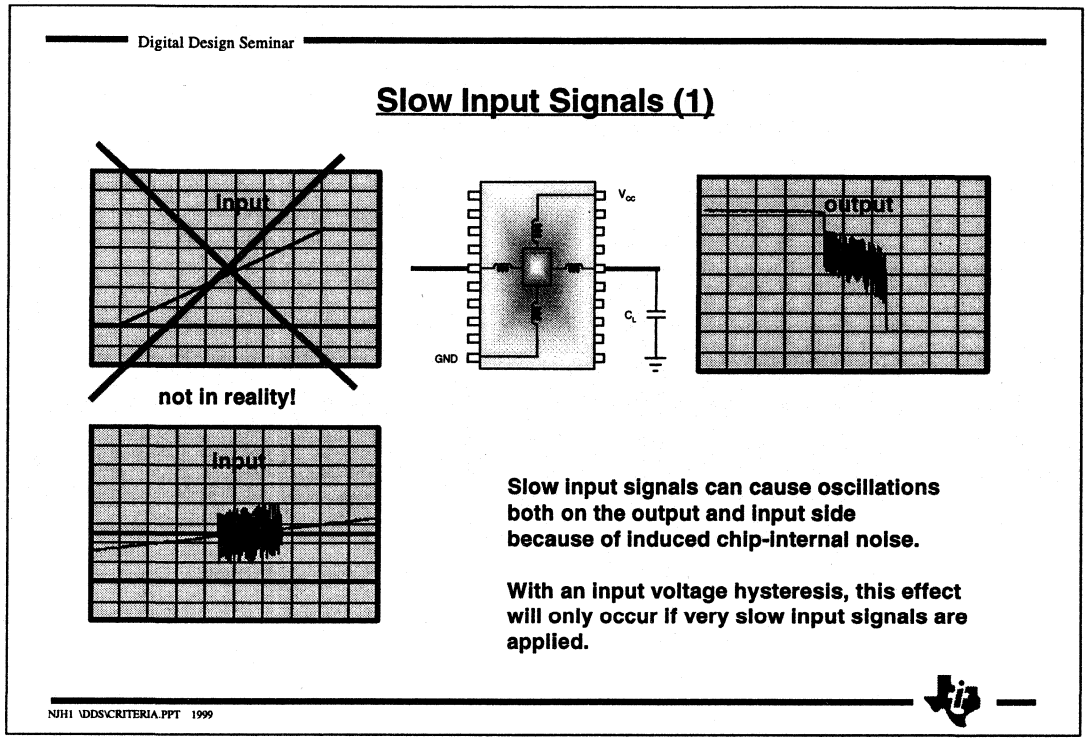
This table shows the propagation delay, tpd, voltage swing, (VOH - VOL), slew rate, and dv/dt for selected logic families. HC, AHC, ALS, AC, F and ABT operate from a 5V supply voltage, while AHC, LV, LVC, ALVC, LVT and ALVT have a 3.3V supply. The data indicates that tpd and dv/dt show common trends (the shorter the propagation delay, the higher the slew rate). However, there is no direct link between the two parameters. In particular, the fastest family is not the one with the highest slew rate.

This must be considered, especially when designing high speed systems. As will be discussed later in this section, high slew rates are very unfavorable as they cause extra noise through current spikes and over / undershoot. The worst technology in this respect is 5V AC. All of the low voltage technologies have somewhat lower signal slew rates.

It should be especially noted that ALVT, the fastest of all technologies shown, exhibits a comparatively low slew rate. This is due to appropriate circuit design techniques and the SSOP/TSSOP package technology used for these 16- to 20-bit bus interface functions.



A problem often overlooked in system design is the problem of a slow input signal.

When using CMOS inputs especially (i.e. with all CMOS and BiCMOS logic devices), a slow input signal transition can lead to very high supply currents, ICC, or to subsequent oscillations on the circuit's output side.

The reason for this is that in each state - high or low - only one transistor conducts. In the transition stage, however, some current flows in both transistors.

If the voltage at the input rises slowly and if it reaches the value of the threshold voltage, the output then switches rapidly from high to low, as a result of this voltage change the load capacitor starts to discharge. This results in a voltage drop at the internal ground potential of the IC. This in turn causes a reduction of the potential difference between the input and the internal ground potential, which has the effect of reducing the input voltage. The consequence is that the output switches to the opposite logic level. The process repeats, but with reversed polarities. This continues periodically, with the duration of the period determined by the delay time of the circuit.

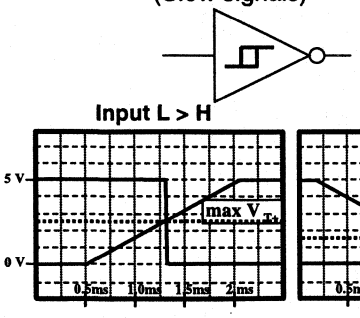
As these oscillations mean high energy moving back and forth between the output and the load, they drastically increase the overall power and heat dissipation of the device. In a worst case scenario, the circuit may be destroyed after some time.

Digital Design Seminar

Slow Input Signals (2)

Schmitt-Trigger Inverter

(Slow signals)



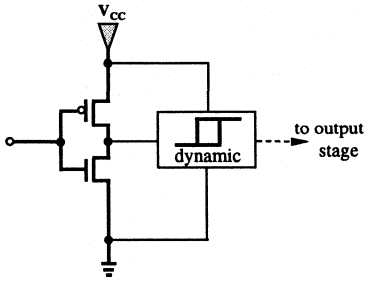
V_{T+} = Positive going input threshold voltage
V_{T-} = Negative going input threshold voltage

Hysteresis : $\Delta V_T = V_{T+} - V_{T-}$ = typically 900 mV

Several Schmitt-Trigger functions available:
SN74AC/T14,SN74AHC/T14,SN74LV,SN74LVC14, SN74LS14,...

Schmitt-Trigger-like inputs

(Edge Noise)



Typical values for Dynamic Input Hysteresis :

ΔV_T (ABT)	= 150 mV
ΔV_T (LVC)	= 100 mV
ΔV_T (ALVC)	= 100 mV
ΔV_T (AVC)	= 100 mV
ΔV_T (LVT)	= 150 mV
ΔV_T (ALVT)	= 150 mV
ΔV_T (LS)	= 400 mV

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Wherever slow input signal slopes need to be processed (e.g for slow signals from peripherals) by logic gates, it is necessary to select those with Schmitt-Trigger inputs, as these have been specifically designed for this purpose.

The principle of a Schmitt -Trigger circuit (shown on the left-hand side of above foil) shows the signal waveforms for a Schmitt-Trigger with an input signal switching within 1.5 ms. The hysteresis can be directly taken from the scope figures.

In the example, V_{T+} , the positive going input circuit input threshold voltage, is at 2.5-V, while V_{T-} , the negative going input circuit input threshold voltage, is at 1.5 V such the hysteresis of the tested Schmitt - Trigger is ΔV_T results in 1 V.

The inputs of the advanced logic families LVC, ALVC, AVC, LVT, ALVT and ABT (and the LS family) are supplied with Schmitt-Trigger-like input stages as the principle on the right side explains.

While the dynamic Schmitt-Trigger-like input circuitry reduces a device's sensitivity to distortions occurring during a rising or falling edge, they are not suitable to handle extremely slow edges. A certain minimum edge steepness is therefore required for these devices. The values listed on the following slide describe an input slope steepness that guarantees proper logic operation for these devices.

SN74ALB-type devices operate with linear circuitry and will exactly reproduce a slowly rising input signal slope at their output. There is no dynamic Schmitt-Trigger circuit at the inputs of the ALB family, as this would make the ALB devices much slower.

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Slow Input Signals (3)

Recommended Input Slew Rate Limits

Series	V_{CC}[V]	$V_{IL,max}$[V]	$V_{IH,min}$[V]	V_T[V]	$T_{f,max}$[ns/V]
SN74	4.74-5.25	0.8	2.0	1.4	100
SN74LS	4.74-5.25	0.8	2.0	1.0	50
SN74S	4.74-5.25	0.8	2.0	1.4	50
SN74ALS	4.5-5.5	0.8	2.0	1.4	15
SN74AS / F	4.5-5.5	0.8	2.0	1.4	5
SN74HC	2.0	0.3	1.5	1.0	625
	4.5	0.9	3.15	2.25	110
	6.0	1.2	4.2	3.0	80
SN74HCT	4.5-5.5	0.8	2.0	1.4	125
SN74AHC	3.3	0.9	2.1	1.5	100
	5.5	1.65	3.85	2.75	20
SN74AHCT	4.5-5.5	0.8	2.0	1.4	20
SN74LV	2.0-5.5	0.8	2.0	1.5	100
74AC	3.0	0.9	2.1	1.5	10
	4.5	1.35	3.15	2.25	10
	5.5	1.65	3.85	2.75	10
74ACT	4.5-5.5	0.8	2.0	1.5	10
SN74LVC	1.65-3.6	0.8	2.0	1.5	10
SN74ALVC	2.3-3.6	0.8	2.0	1.5	10
SN74AVC	1.65-3.6	0.8	2.0	1.5	5
SN74BCT	4.5-5.5	0.8	2.0	1.5	10
SN74ABT	4.5-5.5	0.8	2.0	1.5	5/10
SN74LVT	2.7-3.6	0.8	2.0	1.5	10
SN74ALVT	2.3-3.6	0.8	2.0	1.5	10

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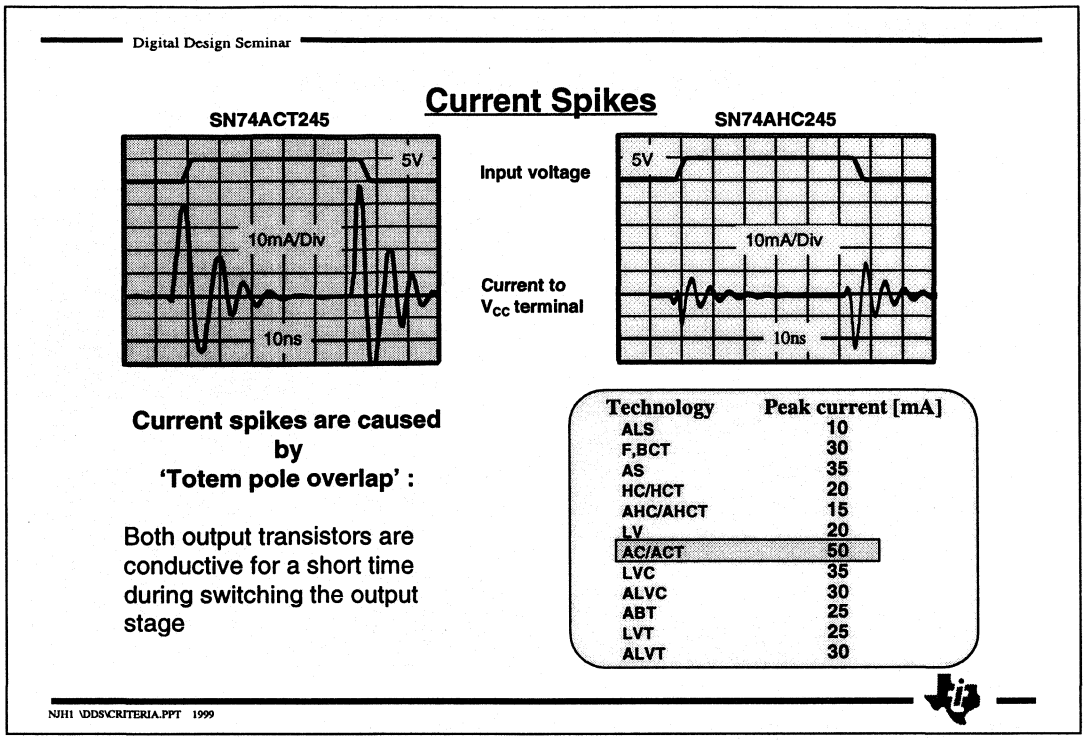
The table above gives an overview of Texas Instruments' logic families with respect to the maximum input transition rise or fall rate.

There is a direct correlation between speed and the parameter for rise and fall time. The faster the family, the higher the rise or fall time and more critical the slew rate.



This foil explains the current peaks which always occur during switching.

A characteristic common to all Totem-Pole and 3-state output stages is an additional current transient, when the output changes from a logic low to high and vice versa.

The internal output circuitry of the devices consists of two alternately conducting transistors. At every transition from logic high - state to logic low - state both output transistors are - for a very short time - conductive. This is called ' Totem pole overlap'.

The total supply-current spike is a combination of three major effects:

- the difference in high-level and low-level supply current
- the charging of load capacitance
- the conduction overlap.

The charging of load capacitance in most cases overshadows the other two effects with respect to noise produced on the supply voltage lines by switching current transients. However, to keep the current spike as low as possible, it is important to maintain low impedance of the power lines. Therefore, a decoupling capacitor (bypass capacitor) at the devices' supply pins should be used and the area covered by the power traces should be kept small.

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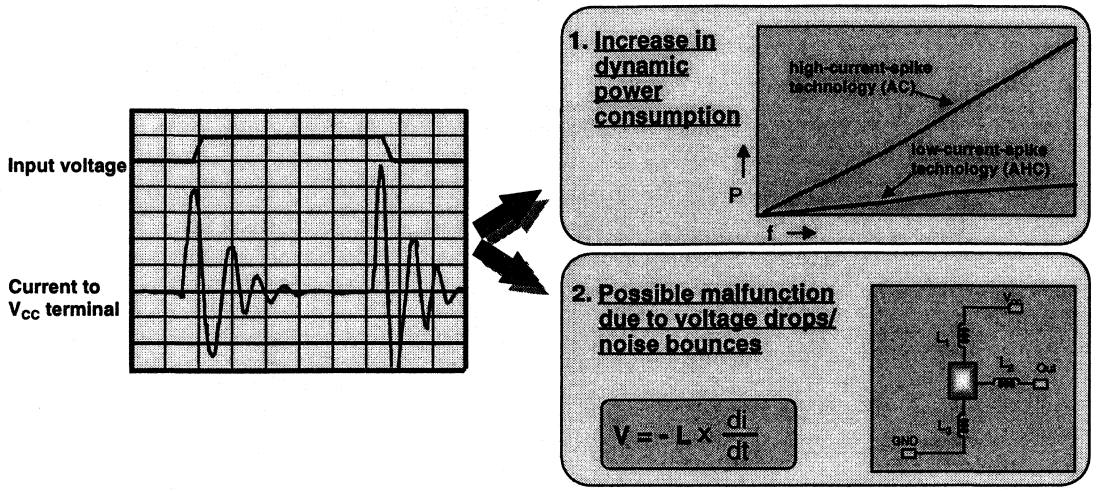
Effects of Current Spikes (1)



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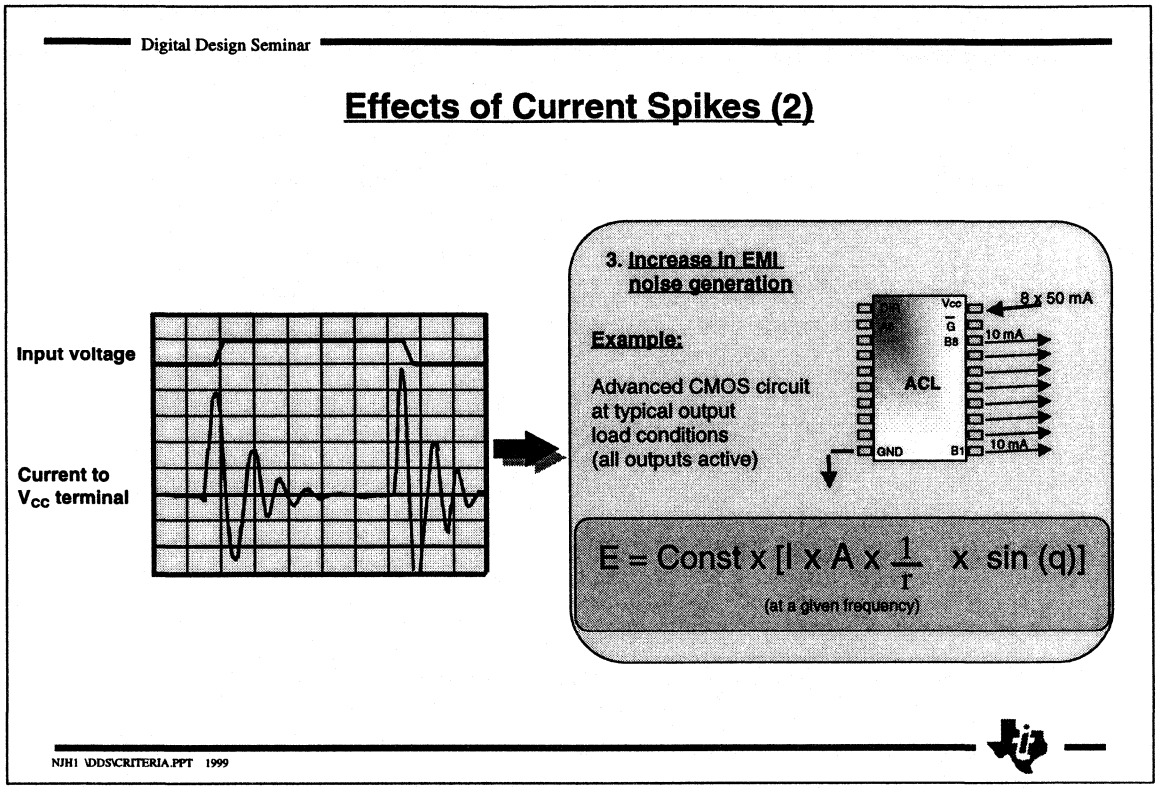
The current spikes at the V_{CC} terminal lead to a higher power dissipation. The power consumption increases proportional to the operational frequency.

The possible malfunctions can be forced by high current deltas on the supply lines related to the given formula.



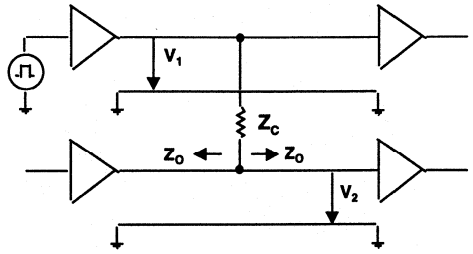
The formula shows that the current peaks are the chief device parameter in the formula of the EMI radiation. All other parameters are either constants or parameters which the designer may consider in PCB layout.

(See details in the EMI section).

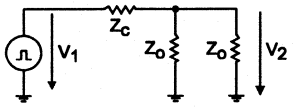
Digital Design Seminar

Crosstalk

On long transmission lines ($2\tau > t_r$) the Crosstalk can be calculated as follows :



Z_o = Line Impedance
Z_c = Coupling Impedance



Crosstalk : $C = \frac{V_2}{V_1} \times 100\,\%$

$= \frac{0.5\,Z_o}{0.5\,Z_o + Z_c} \times 100\,\%$

$= \frac{1}{1 + 2 \times Z_c / Z_o} \times 100\,\%$

Note: At the end of an unterminated line Crosstalk is twice as high (Reflection Factor ρ = 1) !

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When currents and voltages occur on a connecting line in a system, it is impossible for adjacent lines to remain unaffected. Static and magnetic fields interact and opposing ground currents flow, creating linked magnetic and capacitive fields. These cross-coupling effects are lumped together and called crosstalk.

The coupling from the sending line to the receiving line can be represented by taking the coupling impedance Z_C into account. The voltage at the sending line is the voltage source V_1. V_1 is then coupled to the receiving line via the coupling capacitance Z_C, where the impedance looking into the line is the line impedance in both directions.

The voltage impressed on the receiving line (V_2) then propagates along the receiving line to the input of the receiver, which, in case of an unterminated line, can be considered as an open line and voltage doubling occurs.

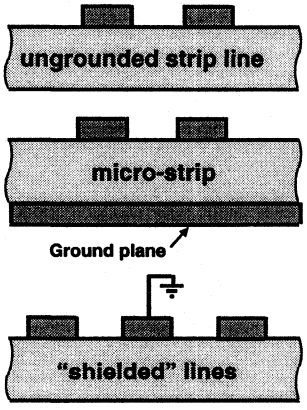
The term V_2 / V_1 can be defined as the cross-talk coupling constant.

The worst-case for signal line cross talk occurs when sending and receiving lines are close together, but widely separated from a ground return path. The lines then have a high characteristic impedance and a low coupling impedance (the lower the coupling impedance, the higher the cross talk constant!).

The next page shows some cross talk examples of typical lines used in digital systems.

Digital Design Seminar

Crosstalk on Printed Circuit Boards (typical Values)



	Line Impedance Z_o [Ω]	Coupling Impedance Z_c [Ω]	Crosstalk [%]
ungrounded strip line	200	100	50
micro-strip	80	125	25
"shielded" lines	100	400	11

Note: line width = line distance

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Crosstalk on a printed circuit board is a function of the mutual reactances (Z_C) and the line parameters which define the line impedance (Z_O). Therefore the coupling constant will vary with the type of transmission line used.

The use of **ungrounded strip-lines** (see figures on foil) is a simple and low cost method, but it is also the poorest for noise rejection.

A **micro-strip** line as well as a **strip line with an adjacent ground line** (middle and bottom values) is, by definition, a conductor placed relatively close to a ground plane/line. Because of the low line impedance and shielding characteristic of the grounding plane/line, its crosstalk is minimal and not a problem with most logic families.

The data shown above can be used to estimate the typical crosstalk effect in digital systems.

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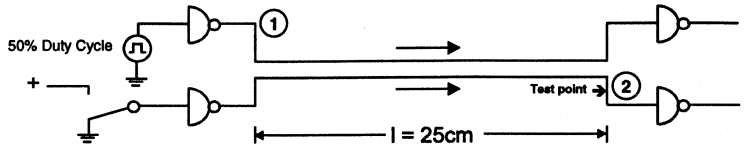
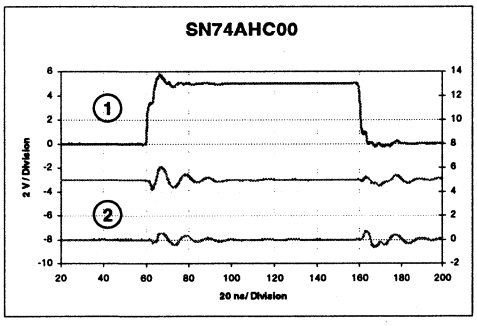
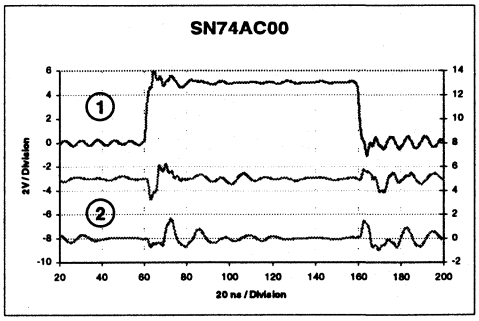
CMOS Logic Crosstalk (1)







Crosstalk between **ungrounded, same-direction** transmission lines is not **critical** when using **AHC**, but becoming **critical** when using **AC(T)** !

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This and the following 4 pages show some practical examples of cross-coupling effects.

In this test circuit, High-Speed CMOS (HC) and Advanced CMOS (ACL) technologies were used. The measurements were taken at a frequency of 5 MHz and a duty cycle of 50%.

ACL, with its high slew rate, has steeper edges than AHC and is a good example to demonstrate crosstalk problems in digital systems.

This foil shows the crosstalk between two ungrounded strip-lines of 25 cm in length with data transmission in the same direction!

Crosstalk between same-direction transmission lines is not critical, when using AHC (as well as all bipolar, BiCMOS and low-voltage technologies), but is somewhat more critical, when using Advanced CMOS technologies (AC/T)!

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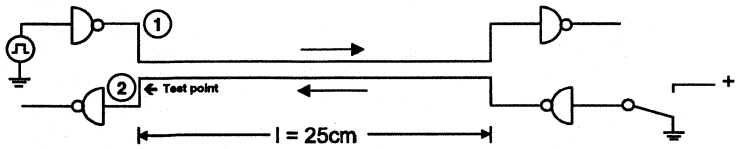
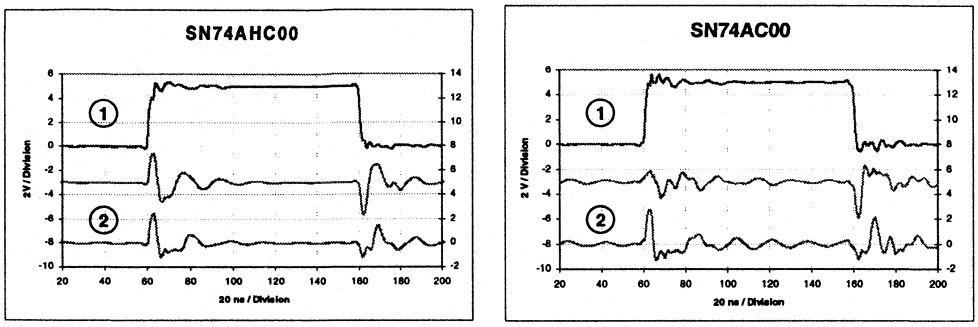
CMOS Logic Crosstalk (2)





The **worst case** scenario for **crosstalk** is between **ungrounded, opposite-direction** transmission lines. Using **AHC** is somewhat **less critical** than using **AC**. But **be careful** when using **5-V CMOS** devices with **TTL - input** margins,
e.g. AHCT and ACT(!). **Highest crosstalk noise** was measured for **AC(T)** circuits !

This foil shows the crosstalk between two ungrounded strip-lines of 25 cm in length. It is important to notice that now the lines use the opposite transmission direction. Opposite-direction transmission is worse than same-direction transmission!

Crosstalk between opposite-direction transmission lines is less critical when using AHC (and most bipolar, BiCMOS and low-voltage technologies), but be careful when using CMOS devices with TTL input margins (AHCT)!

Very high crosstalk noise is caused when using AC(T)! Especially with ACT devices, one may expect malfunctions as a result of the crosstalk noise, because the over- and undershoots may exceed the TTL-input margins of V_{IL} = 0.8 V and V_{IH} = 2.0V significantly.

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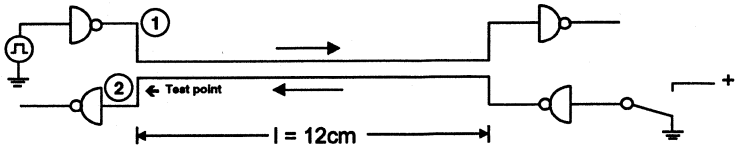
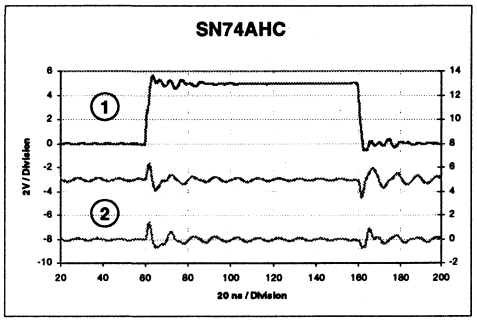
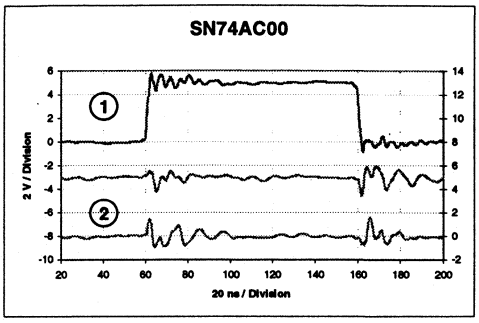
CMOS Logic Crosstalk (3)







Data transmission in **ungrounded, opposite direction** is usually **not critical**, if the lines are **shorter** than **12 cm**. However, **be careful** when using **AHCT/ACT circuits** !

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Crosstalk can be reduced by shortening the length of the adjacent lines.

This foil shows the crosstalk of two ungrounded strip-lines of 12 cm in length. Again, to reflect the worse-case situation, both lines use the opposite transmission direction!

If the lines are shorter than 12 cm, data transmission in opposite direction is usually not critical. However, be careful, when using 5V CMOS circuits with TTL compatible inputs, such as HCT, AHCT and ACT!

The same improvement can be seen if we increase the space between both lines. However, either shortening the line length or increasing the space between the lines is not very effective to reduce crosstalk noise, as this that means changing the layout or even the hardware.

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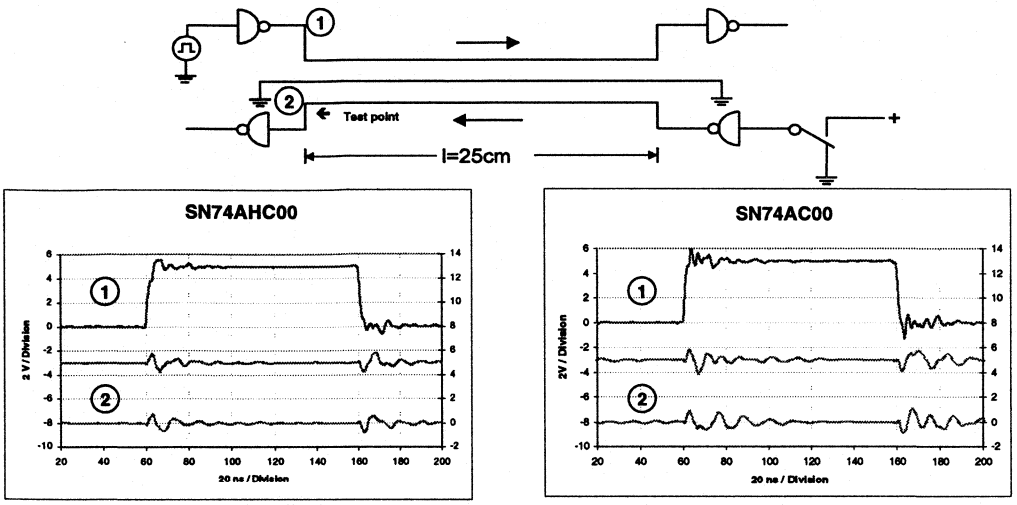
CMOS Logic Crosstalk (4)



By using a **shielding** (GND line between the transmission lines), **crosstalk** can be **reduced to an uncritical level**.

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A more effective method to minimize crosstalk noise is to use a shielding line (ground line) between the adjacent strip-lines.

This foil shows the crosstalk of two strip-lines of 25 cm in length with a shielding line in between. Also, to show the worse-case scenario, both lines use the opposite transmission direction!

By using a shielding line (grounding on both sides is advised), crosstalk for all logic families can be reduced to an uncritical level - even with 5V CMOS circuits with TTL compatible inputs (HCT, AHCT and ACT).

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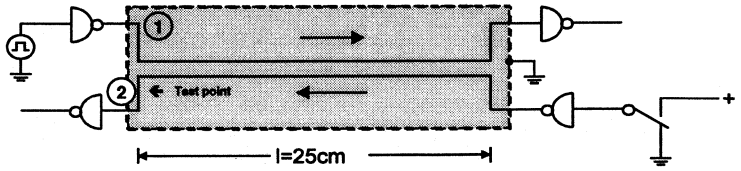
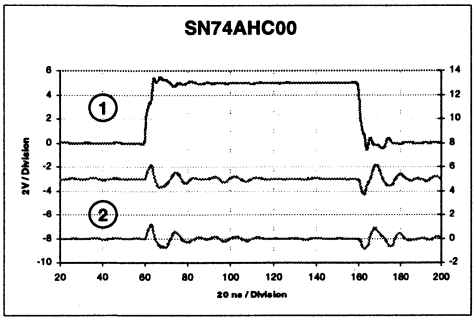
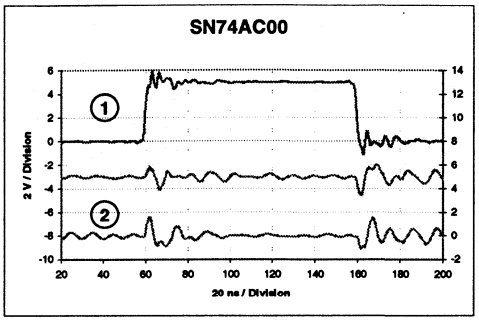
CMOS Logic Crosstalk (5)







Crosstalk on **opposite-direction** transmission lines over a **ground plane** (micro-strip) **is not critical** in most cases.

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The same improvement demonstrated by the shielding line can be seen if we use a ground plane underneath the adjacent signal lines. Even if the crosstalk constant is slightly worse than with the shielding line, it effectively eliminates crosstalk in most cases.

All the considerations regarding the crosstalk shown on this and the previous foils, were related to two layer boards. However, using two layer boards the distance between ground- and signal lines is relatively large.

Nowadays most of the new applications are done using multi-layer PCBs.

With the multi-layer boards there is a smaller distance between the signal- and and the ground- traces so that the crosstalk is further reduced.

Digital Design Seminar

Circuit Speed vs Slew Rate: Overview

	HC	AHC	AC	F	ABT	LVT	LVC	LV	ALVC	ALVT
Propagation Delay [ns]	9.9	4.0	4.1	3.6	2.9	2.4	4.1	8	2.1	1.5
Voltage Swing [V]	4.8	4.8	4.8	3	3	3	3	3	3	3
Slew Rate [V/ns]	0.9	0.8	1.8	1.3	1.0	1.2	0.9	0.7	1.3	1.4
Crosstalk Noise	medium	medium	high	medium	medium	medium	medium	low	medium	medium
Recommended PCB	2-layer	2-layer	Multi-layer	Multi-layer*	Multi-layer	Multi-layer	Multi-layer*	2 - layer	Multi-layer	Multi-layer
Current Spike [mA]	20	15	50	30	25	25	35	20	30	30
Number of ICs per Gate	n = 4	n = 4	n = 1	n = 2	--	--	n = 2	n = 4	n = 2	--
Blocking Capacitor Bus Driver	n = 2	n = 2	n = 1	n = 1	n = 1	n = 1	n = 1	n = 2	n = 1	n = 1

n = number of devices per decoupling capacitor

* 2 layer accepted in safe systems

★ **Example:** '244 function ('16244 in case of ALVC), outputs loaded with 50 pF; all values are typical

★ Slew rate values shown are the higher ones of rising and falling edge of output signal

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This table summarizes different noise types, noise sources and some methods of controlling them for selected logic families.

Critical noise sources are the propagation delay, t_{pd}, voltage swing, (V_{OH} - V_{OL}), slew rate, dv/dt and current spikes. HC, AHC, AC, F and ABT are operating from a 5V supply voltage, while LV, LVC, ALVC, LVT and ALVT have a 3.3V supply.

The data indicate that t_{pd} and dv/dt show common trends (the shorter the propagation delay, the higher the slew rate). However, there is no direct link between the two parameters. In particular, the fastest family (ALVT) is not the one with the highest slew rate.

Crosstalk will be worse in the case of opposite-direction transmission lines. Solutions are to use shielding lines or separate ground and V_{CC} planes with multilayer boards. In the latter case it should be noted that crosstalk may still in some cases be critical with ACT or other fast TTL-compatible CMOS parts.

Current spikes are one of those effects which apply to more or less all digital circuits. While the effects of supply voltage drop effects can be addressed by appropriate design (e.g. by using a GND and V_{CC} plane and a bypass or a decoupling capacitor), both the increased dynamic power consumption and the increased EMI noise energy are device-related effects. Therefore a system designer's only option is to choose appropriate technologies that have low current spikes.

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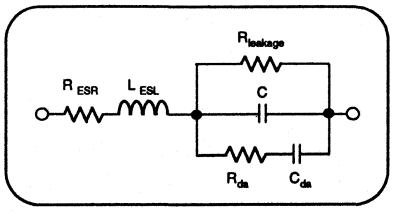
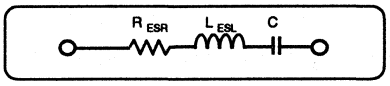
Decoupling Capacitor

Model of a 'Real' Capacitor

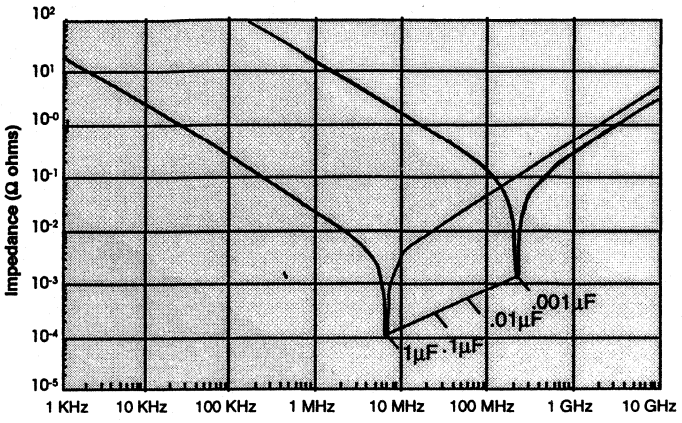


First Order Approximation



R_{ESR} = Equivalent Series Resistor
L_{ESL} = Equivalent Series Inductance
R_{DA} = Dielectric Absorption Resistor
C_{DA} = Dielectric Absorption Capacitor

Typical Resonant Graph
for various size capacitors*



* SPICE SIMULATION RESULTS
assumptions : $R_{ESR} = 1e^{-4}\ \Omega$ (constant)
$L_{ESL} = 5e^{-10}$ nH (constant)

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Unlike an 'ideal' capacitor, a 'real' capacitor is characterised by additional 'parasitic' inductances, capacitances and resistances.

The capacitor model as well as its first order approximation are shown in the figure.

The parasitic elements are resistive and inductive elements, non-linearity, and dielectric memory. The resulting characteristics composed of these elements are generally specified on the capacitor manufacturer's data sheet.

The effects result in resonant characteristics as shown in the graph: the impedance of the capacitor will greatly vary over frequency, thus forcing the designer to consider carefully the frequency range and blocking currents needed, and then choose the capacitor accordingly.

Bypassing a power line (or plane) from the device internal noise requires capacitors with very small inductance. An appropriate choice for HF decoupling is a monolithic ceramic -type capacitor or the multi-layer ceramic chip capacitors (MLC) , which have very low series inductance.

For this reason they are more suitable than electrolytic, paper or plastic film capacitors, which basically consist of two sheets of metal foils separated by sheets of paper or plastic dielectric and formed into a roll. These capacitors are only suitable for very low frequencies and perform more like a inductor than a capacitor at frequencies just slightly above a few MHz.

Ceramic type capacitors exhibit negligible internal inductances, thereby allowing the charge to flow easily when needed without degradation.

For TTL and CMOS systems, a good guideline is 0.01 µF to 0.2 µF per device.

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Decoupling Guidelines

★ **Capacitance can be calculated**

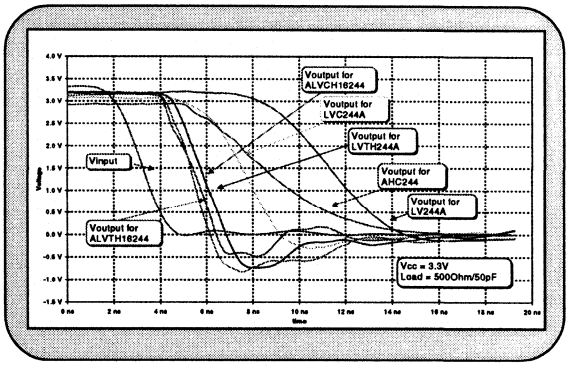
$$I = C \times dv/dt,$$

$$\Rightarrow C = I \times \Delta t / \Delta V$$

from the amount of current needed, how long the current is needed and what change in voltage is acceptable

★ ***Rule of thumb:*** **Choose a capacitor whose resonant frequency is at least as high as the corresponding edge rates of the switching signals, where frequency response at**

$$f = 1 / (3.5 \times t_{rise,fall})$$



$$f_{res}(LVC) = \frac{1}{(3.5 \times 2ns)} = 143\ MHz$$

★ **Place the capacitors as close to the switching device as possible. In the case of a transceiver place the capacitance between the V_{CC} and Ground planes at the device. In the case of termination place the capacitance from the supply voltage to Ground at the termination resistor.**

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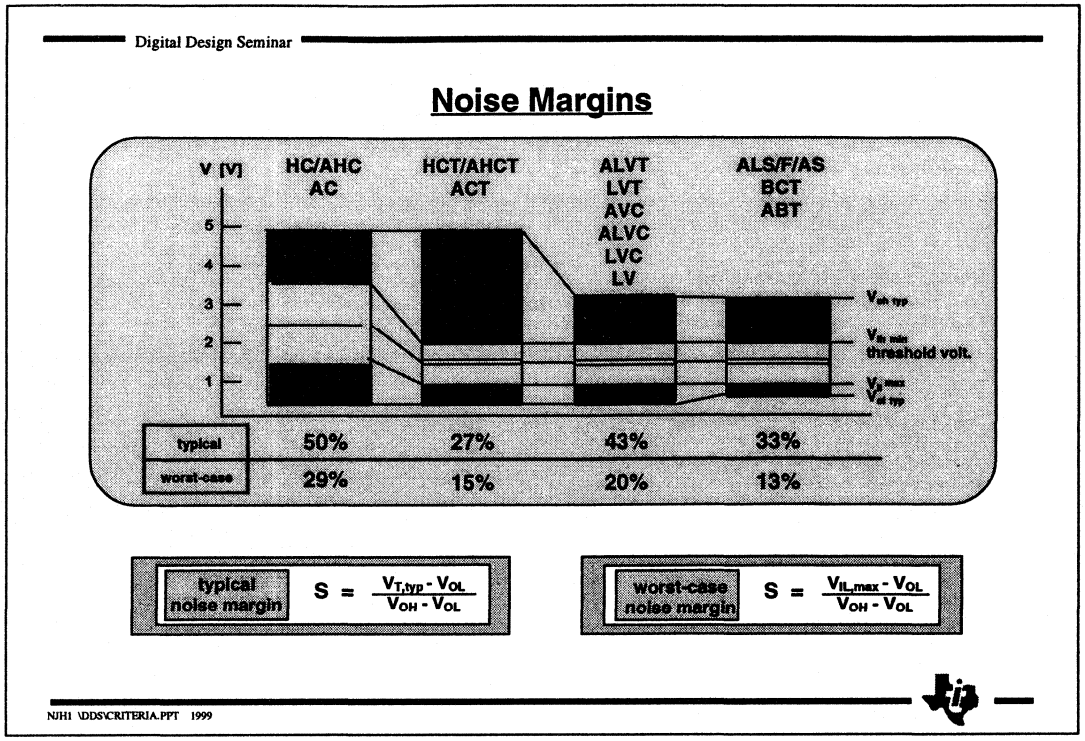
While the slew rate and the corresponding ground bounce noise mainly depend on the chosen technology, a system designer will have to decide on the decoupling method used to prevent voltage drops and ringing on the power supply lines. This is somewhat more critical in 3.3-V systems than in 5-V environments, where larger voltage drops are still acceptable.

A bypass (decoupling) capacitor stores the electrical energy that is released to the power line whenever a transient voltage spike occurs. It provides a low impedance supply, thereby minimizing the noise generated by the switching outputs of the device.

For effective decoupling on printed circuit boards the most desirable arrangement is a multilayer board with solid GND and VCC plane.

Another thing to remember about high frequency is the actual physical placement of the capacitor. Even short lengths of traces have considerable inductance, so the bypass capacitor should be placed as close as possible between the power pins of the device, and leads should consists of short, wide PC tracks.

The best way to ensure decoupling at both high and low frequencies is to use an electrolytic-type capacitor, such as a tantalum bead, in parallel with a monolithic ceramic one. The combination will have high capacitance at low frequency and will remain capacitive up to high frequencies. It is generally not necessary to have the tantalum capacitor at each IC. It is acceptable to share one tantalum capacitor between several ICs if the reasonably wide track is shorter than 10 cm.

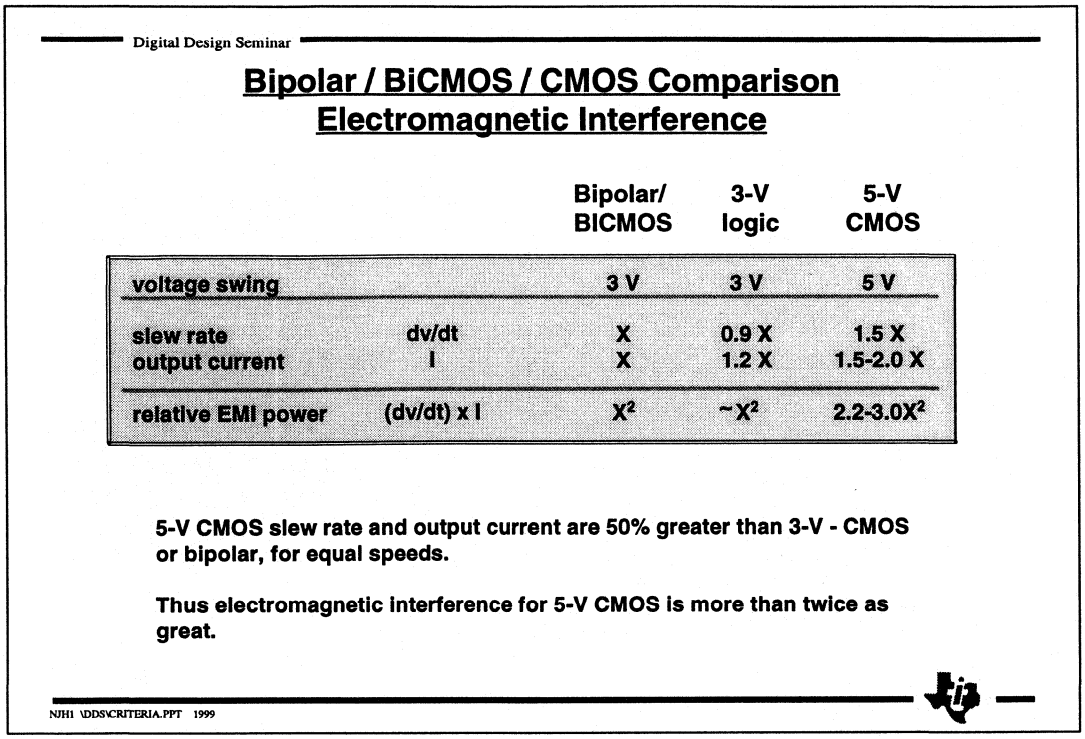


Noise margin is a voltage specification that ensures the static DC immunity of a circuit to adverse operating conditions. The noise margin is defined as the difference between the worst-case input logic level and the worst-case output logic level.

The usefulness of noise margins at the system design level is the ability of a device to be resistant to noise spikes at the input.

The above comparison shows the noise margin for selected logic families. The 5V CMOS families - HC, AHC and ACL - have a typical noise margin of 50% and even in the worst-case condition a remarkable noise margin of 29%. In comparison, the TTL-compatible Bipolar and BiCMOS families have only 13% in the worst-cast condition. But if we have a look at the low-voltage families, all 3.3V devices have an improved noise margin of 20% in the worst-case, which makes this families even more attractive for new designs.

The improved noise immunity of 5V CMOS and 3.3V families over bipolar and BiCMOS devices is due to the rail-to-rail (V_{CC} to GND) output voltage swing. This noise immunity makes them ideal for high noise environments. However, keep in mind that TTL-compatible 5V CMOS devices, such as HCT, AHCT and ACT, have similar noise margins to Bipolar and BiCMOS.

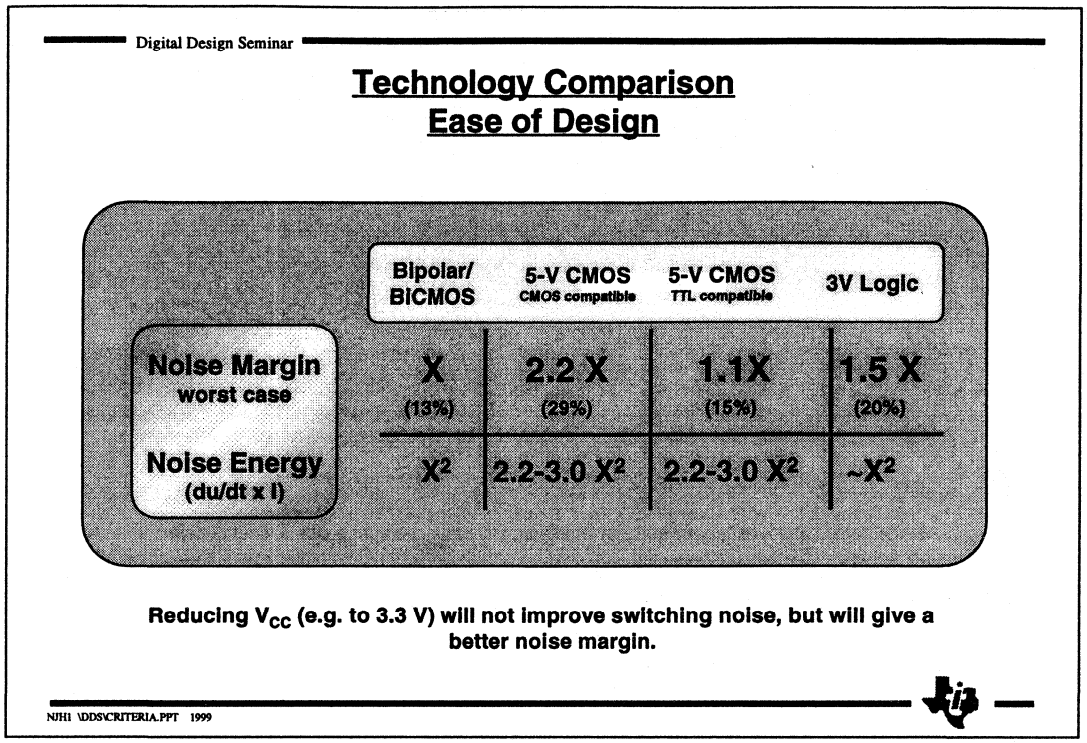


Like line reflection, crosstalk or simultaneous switching, noise from Electromagnetic Interference (EMI) depends on the integrated circuits switching characteristic.

The three major factors affecting EMI are the output voltage swing, the devices' slew rate and the output current. However, all three factors can be addressed to minimize switching noise:

- Output Edge Control™ (OEC) reduces high-frequency components (implemented in all new logic families at TI)
- lower output voltage swing - this reduces critical slew rate (e.g. use 3.3V logic)
- reduce package inductance (SOICs better than DIPs)
- minimize output drive (e.g. use AHC instead of ACL)

As a result from above calculation, the EMI noise from 5V CMOS is more than twice that of bipolar or 3.3V devices.

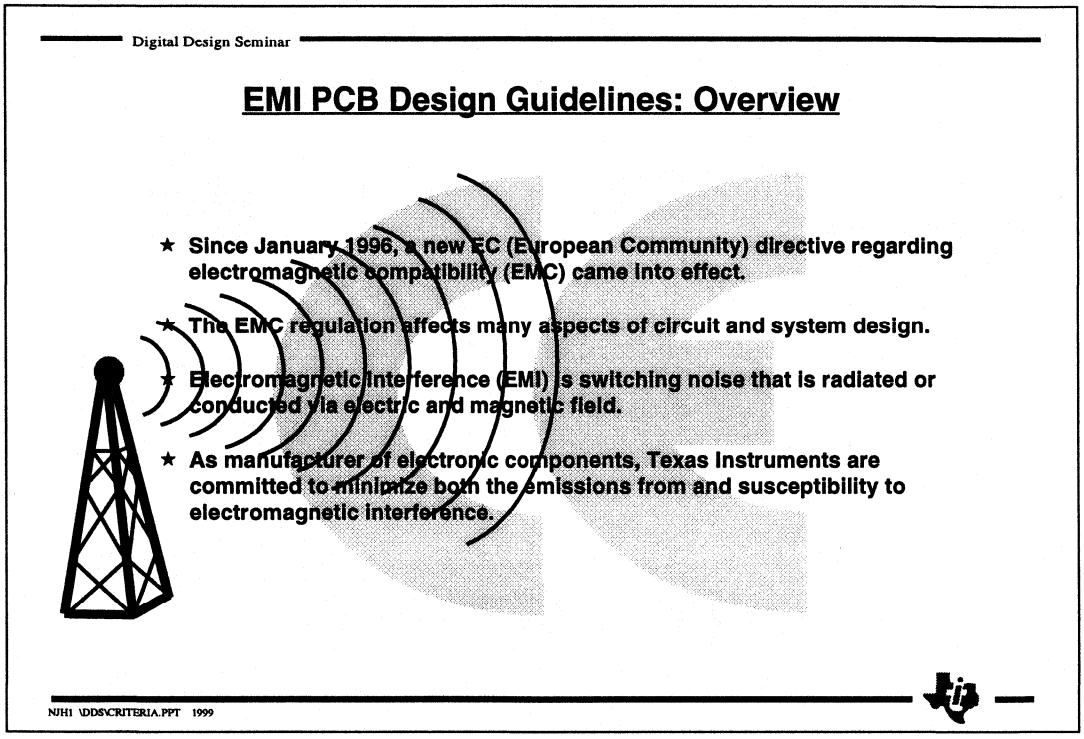


A general technology comparison between Bipolar, BiCMOS, 5V CMOS and 3.3V CMOS circuits will only make sense if both the device-related noise energies and the noise margins that are dictated by the input and output signal level specifications are considered.

Looking at these two parameters, one finds that Bipolar or BiCMOS circuits show about the same 'ease of design' as CMOS parts working at CMOS levels (ie with a VCC/2 input threshold voltage).

Looking at the 3.3V technologies you actually see the best ratio in noise energy vs. noise margin, which in addition makes 3.3V devices very attractive for new designs.

The **most critical combination**, however, is CMOS process technology and bipolar-like TTL-level specifications. Because of high noise levels of CMOS and the lower noise margins of TTL-level systems, a crucial obstacle can be encountered if developing reliable systems.

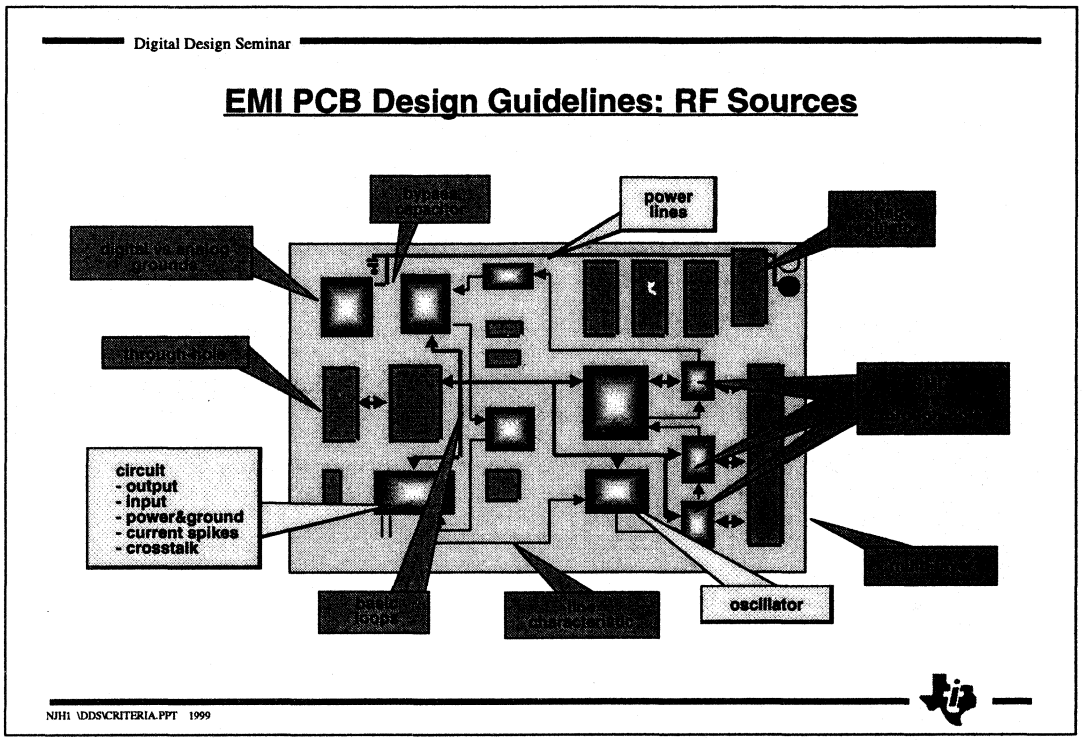


The EC (European Community) regulations regarding EMC will affect many aspects of circuit and system design. However, there are many considerations that can be applied generally to reduce both the emission from and susceptibility to EMI.

Electromagnetic interference (EMI) often seems like a mysterious phenomenon. EMI can be difficult to control, and even the results of EMI testing can vary from day to day and from test facility to test facility. At times, the act of controlling EMI has been called "black magic" or "voodoo". However, EMI has been researched for many years, and guidelines have been established that can improve the electromagnetic compatibility of a system to which they are applied.

Designing for low EMI from the start of a project results is much easier and less expensive solutions than attempting to fix EMI problems after a design has reached the testing phase of development. Consequently, following a few guidelines for printed circuit board (PCB) design at the beginning of a project can help to minimize the system's EMI while adding little or no cost to the system.

This chapter will give some tips and recommendations for low-noise design.



Let us start looking at typical digital PCB with a quick look at the most EMI critical areas on the PCB.

There are **three** important contributors of RF noise.

The number one problem is noise from the IC I/O pins, simply because the area covered by traces connected to them on the PCB makes a large antenna (basic loops!).

The second most important contributor is the power supply system which includes the voltage regulation, the bypassing capacitor and the supply lines. These 'components' are the source and the sink of all RF energy in the system.

The number three noise source is the oscillator circuit, where the oscillator swings rail to rail. In addition to the fundamental frequency, harmonics are introduced on the output side.

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EMI PCB Design Guidelines: Definition

RF-Source:	**Trace bound (RF-voltage/current) and radiated interface (RF- noise), e.g. active components like diodes, transistors, integrated circuits, etc.**
RF-Channel:	**Signal lines; power lines; boards; modules; systems**
RF-Sink:	**Receiver of RF-noise (e.g. IC input, IC supply-pins)**
RF-Noise:	**Caused by voltage, current or field effects --> important factors are amplitude and period**
RF-Effects:	**Reflection; cross talk; current spikes; simultaneous switching; coupling of signals; etc.**

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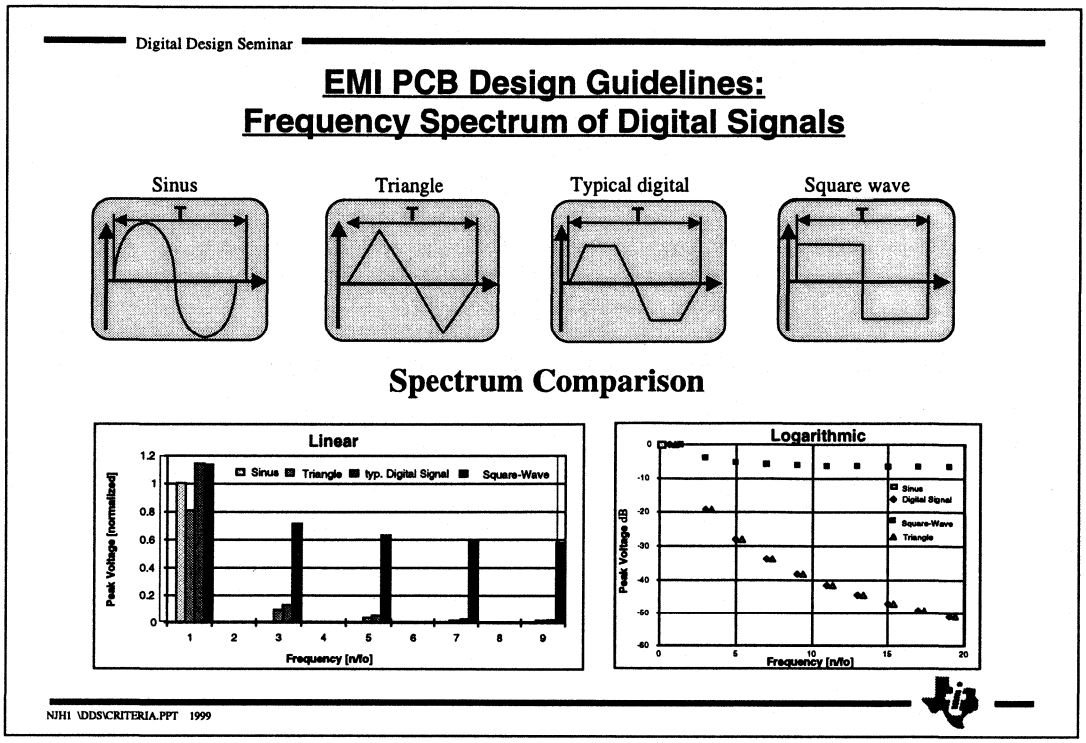
EMI requires a source, a path and a receiver. In today's electronics, integrated circuits (IC) often supply the source and the printed circuit board, as well as the associated cabling and wire harness. These act as the conductive and radiating part of the path, otherwise called the antenna. The receiver simply can be a IC's input, a sensitive electronic module, such as a radio, or it can be a loop at the PCB, accidentally designed to receive electromagnetic noise.

EMI generation is a function of RF-source, RF-channel and RF-sink. All three 'components' are involved in EMI generation in a system, as they source, transmit and feed the current required in switching.

The two major factors affecting RF energy are the amplitude and period of the switching signal: Switching frequency, duty cycle, edge rate, noise content and voltage levels.

Noise is generated and coupled out through many different possible mechanisms: line reflection, crosstalk, current spikes, simultaneous switching, etc.



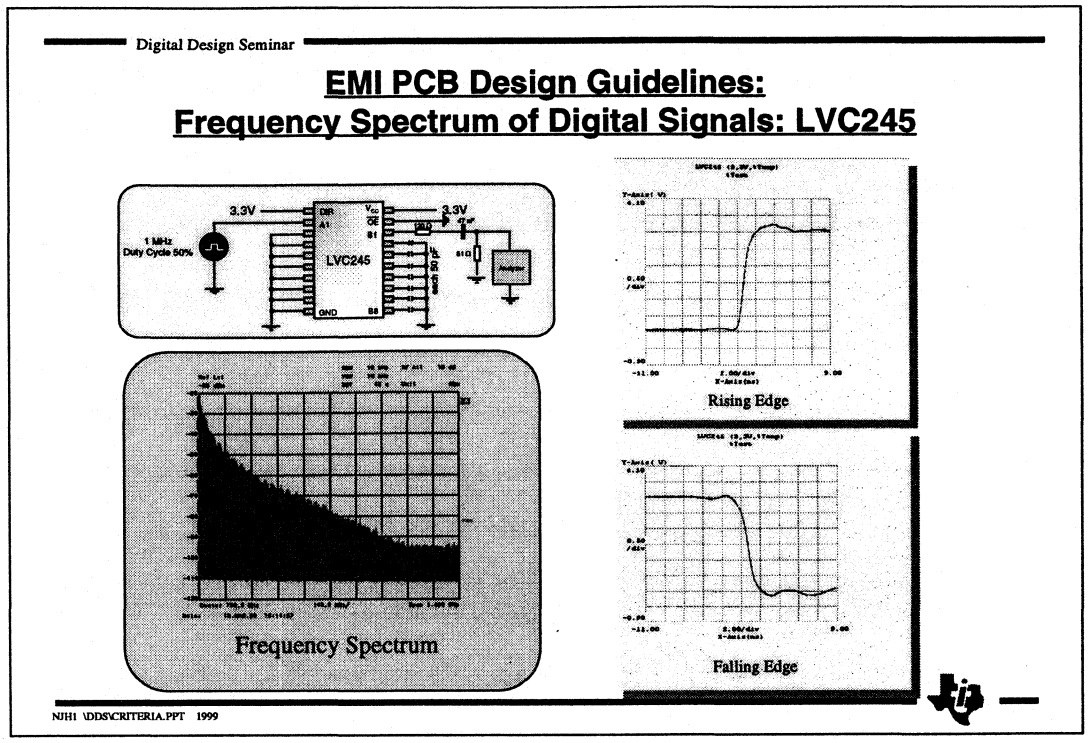
To get a better understanding of EMI, it is important to know the frequency spectrum of the waveform used in digital systems.

The upper curves represent some basic signal waveforms which could be found in today's electronic systems. In digital systems, however, the trapezoidal (square) signal dominates. Apart from the sine waveform, all the others include beside the fundamental frequency, also harmonics.

The fundamental frequency and its harmonics, as well as any noise (ringing) on the signal, will influence the frequency envelope in which EMI generation may be expected.

The lower curve illustrates the theoretical spectral lines of the upper signals.

The sine curve consists of only one spectral line, whereas the square wave includes a lot of high frequency harmonics. The right-hand figure illustrates the logarithmic spectral content in dB.



The above slide illustrates a lab measurement of output spectral content for SN74LVC245.

The measurement setup represents a typical bus line with about 150 Ohm resistance and 47 pF capacitance.

The spectrum of the digital signal was measured with a spectrum analyser at the end of the artificial bus line.

The shape of the spectrum envelope shows good conformity to the theory. At this point you should not forget that the spectrum is given in dB (20 dB are equal to factor 10 !)

The figure on the right-hand side shows the output signal of the SN74LVC245.

The slew rate with this test condition is about 1.5V/ns and the rising and falling edges are very symmetrical.

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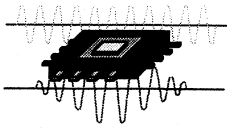
EMI PCB Design Guidelines: IC-I/O Pin Noise

★ The number one problem is RF-noise from the IC - I/O pins

- signal/power traces connected to the pins on the PCB make a large antenna



★ Noise from a pin is a function of the chip and package

- minimize output voltage swing	→ e.g. 3.3V logic
- reduce package inductance	→ SOICs are better than through-hole devices
- smooth output waveform edge	→ use devices with Output Edge Control ™
- minimize capacitive loading	→ reduces current loading per part
- eliminate switching noise	→ use bypass capacitor, advanced packages, avoid undefined input voltages
- minimize output drive	→ e.g. use AHC instead ACL

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RF noise from the device is a major concern for circuit board design. That noise is generated internally in the device and is coupled out through many different possible mechanisms.

The noise will be present on all outputs, inputs, and power and ground, at all times. Basically, every pin on the device could be a problem.

The most critical pins are the IC I/O pins, simply because the area covered by traces connected to them on the PCB makes a large antenna. The noise from clock switching internally to the IC, simultaneous switching, internal crosstalk or current spikes, appears as noise spikes on outputs and inputs as well as power/ground pins.

At the chip and package level several design improvements have improved signal quality. Additional internal circuits like Output Edge Control™ (OEC), Power-On-Demand (POD), Bus Hold (BH) and package improvements like a split ground lead frame, (thin small-outline packages), WidebusTM packages and flow-through pinout, help to minimize device-generated noise.

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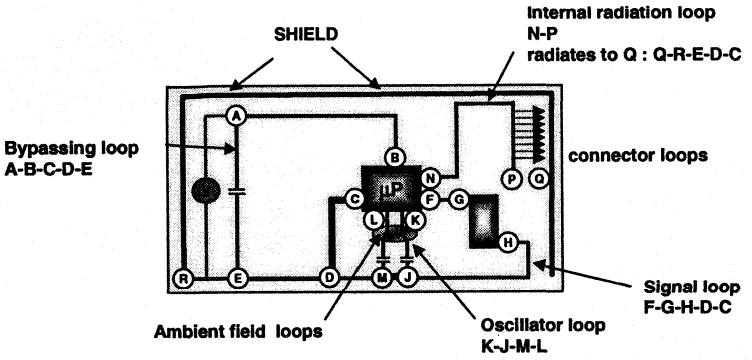
EMI PCB Design Guidelines: Basic Loops

★ Every signal sent out from the IC to another chip returns on the *return path* back to the IC (e.g. via ground)
- ★ It travels in a loop back to where it originates
- ★ loops are antennas which radiate RF energy



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The amount of radiation produced by an electronic system is to a large extent proportional to the efficiency of its radiating antennas - or basic loops. Antennas or loops on a PCB include all traces, components, component leads, connectors and wiring harnesses.

Every edge transition that is sent out from the μP to another chip, is actually a current pulse. It goes to the receiving device and actually exits through that device's ground pin. It then returns, via ground traces, back to the ground pin of the μP. It travels in a loop back to where it originates.

Loops exist everywhere. Any noise voltage and its associated current will travel the path(s) of lowest impedance back to the place where it was generated.

A loop can be a signal and its return path, the bypassing loop between power and ground and the active device inside the μP, the oscillator crystal as well as the loops from power supply or voltage regulator to bypassing caps. Other more difficult loops are actually ambient field loops. For example, the crystal itself radiates and can be coupled into a wire running nearby. Then the wire contains noise that is going to try to get back to the crystal loop. That may mean a very long convoluted path, which of course serves as another antenna for the crystal noise.

The understanding what loops are is a very powerful concept, because it allows us to track all the signals on the board, to avoid unknown return paths (flying leads) and to change noise propagation by controlling the shape and impedance of the return path.

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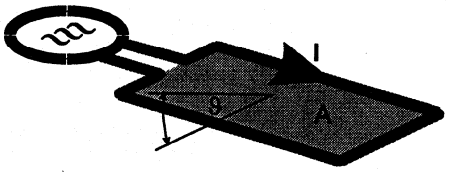
EMI PCB Design Guidelines: Antenna radiates RF noise

★ **Loops and dipoles are antennas. Their radiating efficiency increases up to 1/4 wavelength of the frequency of interest,**

★ **at**

- ⇨ **1MHz, λ/4=75 meters *)**
- ⇨ **300MHz, λ/4=25 cm *)**



★ **Normally, trace length becomes important when greater than**

- ⇨ **λ/10: Federal Communication Committee (FCC) Limits**
- ⇨ **λ/20: Automotive**
- ⇨ **λ/40: Mil Std**

$$E = k \cdot I \cdot A \cdot \frac{1}{r} \cdot \sin \vartheta$$

*) vacuum; effective length of the antenna is determined by μ_r and ε_r (PCB ε_r=5)

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Loop areas can be the most serious EMI threat. A loop can transmit as well as receive electromagnetic energy. Thus, the loop areas associated with a PCB directly affect the emissions and immunity of the system.

Loops and dipoles are antennas. As the size of a loop increases, so does the efficiency of the loop as a radiator. The radiating efficiency increases up to 1/4 wavelength of the frequency of interest. Geometrically, that means, in case of a loop, that the larger the laid-out area of the loop, the stronger the radiation. This is true until one or both legs of a loop reach 1/4 wavelength.

Thus to minimize radiated and received EMI, loops must be made as small as possible.

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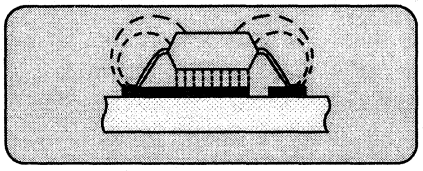
EMI PCB Design Guidelines: Power & Grounds (1)

★ The power supply system is often the most important contributor of RF noise (Current spike)

★ Ground & Power should have an inductance as low as possible
- 2-layer board: length to width ratio should not exceed 3:1 (bypass capacitor)
- power and ground should be run directly over each other (Z ; loop-area)

★ A 2-layer board can achieve 95% of the effectiveness of a multi-layer board, if you:
- route the ground underneath power
- grid the power and ground
- route return path directly under/parallel the signal trace (gridding; ground plane)
- build a solid plane for ground under the IC



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Proper power routing is of fundamental importance to achieve electromagnetic compatibility. The only non-DC current that should flow in the power lines of the PCB is the current for the bypassing capacitor. High-frequency current used inside the IC should come from the bypass capacitor, not the power supply!

Since a "ground" is really a current return path in most cases, the goal of any trace carrying RF energy is to provide the lowest impedance current path possible without generating additional noise. A ground (power) plane will best accomplish this task. However, also a ground grid for digital circuitry can provide low-impedance signal return paths on a two-layer board and does not require the additional cost of a ground plane.

Power should be routed over (under) or next to the ground, whenever possible. The power lines typically contain the most high-frequency noise in a digital system. Therefore routing power directly over ground results in a path with low inductance and minimized radiating loop area. Routing power and ground next to each other is the next best alternative.

Additionally, series filters, such as ferrites or inductors, often prove helpful for reducing noise on power supply routes. A π configuration can be used on the V_{CC} pin. Also, the ferrite should be located very close to the pin of the IC, in order to keep the noise off the PCB trace.

A solid ground area under the IC becomes a ground island for the RF noise generated by the IC. It provides a low inductance path and minimizes the radiating loop area. The ground should be connected to IC ground and the bypassing capacitor ground.

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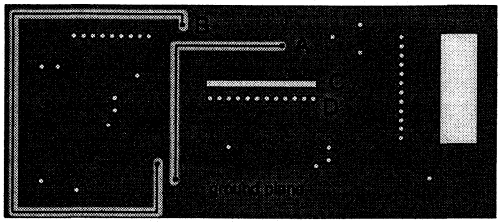
EMI - PCB Design Guidelines: Power & Grounds (2)

★**Multi-layer board**



A: POOR - **buried trace cuts ground plane into two parts**

B: BETTER - **buried trace around the perimeter; best is no trace at all in the ground plane**

C: POOR - **Slot cuts up ground plane, focuses slot antenna radiation into that connection**

D: BETTER - **Ground plane extends between 100 mil centers**

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The closest approximation to having a ground plane in a 2 layer board comes from gridding the ground. The following guidelines are meant to maintain the advantages gained with a ground plane or ground gridding:

- Pay the utmost attention to how the holes and cutouts on planes are done. They break up the plane and therefore cause an increase in loop areas.
- Avoid buried traces in the ground plane. If you have to use them, put them in the upper side of PCB. See A and B in above figure.
- When making through-holes for sockets or connectors in the plane, place a small trace between each pin. Breaking up a plane with a row of holes is much, much better than having a long slot. See C and D in above figure.
- When splitting the ground plane up to make, say, a digital and power ground, make sure that the signals connected to the IC are still located entirely over the digital ground. Extending signals over the power ground hurts, because the power ground does not work to reduce the loop area for digital noise signals.

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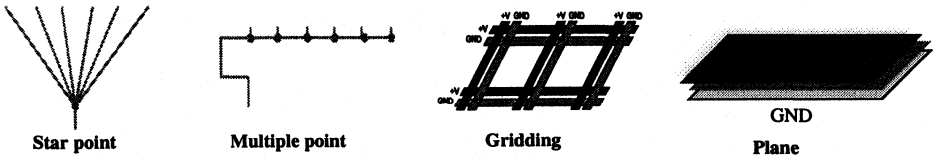
EMI - PCB Design Guidelines: Power & Grounds (3)

★ **Power Distribution**



Star point | Multiple point | Gridding

		Star point	Multiple point	Gridding	Plane V_{CC}	Plane GND
Power lines	digital	fair *	poor	fair	good	good
	analog	good	poor	poor	fair	good
Signal lines	digital	good	poor.. good**	n/a	n/a	n/a
	analog	good	poor	n/a	n/a	n/a

*short traces ** ensure correct termination

In a mixed-signal environment digital and analog parts should be separated from each other and connected only at a low-impedance ground node. This configuration will reduce the coupling of digital noise onto sensitive analog circuitry.

Digital grounds should be designed to return high-frequencies through a low-impedance path, and analog grounds should normally be designed to return low-frequency current or DC to its origin through a low-resistance path.

For digital signals, a ground plane or alternatively a ground grid can provide a low-impedance signal return path for high-frequency noise. Contrary to the star point scheme, the ground grid (plane) is best in order to reduce RF noise and overall costs.

For analog circuitry a star-point grounding scheme is often better, in order to avoid the presence of ground loops. The star point (parallel connection) or the multi-point (series connection) provides the cleanest current return path for analog signals. Star point connection is best, in order to avoid ground loops, but more expensive to design on PCB. Multi-point is less desirable, but easier to design. Thus, a star point should be used for the most sensitive analog signals, and multi-point used for less sensitive analog devices. Star point grounding is also preferred for noisy or high-power circuitry.

Digital Design Seminar

EMI - PCB Design Guidelines: Board Zoning

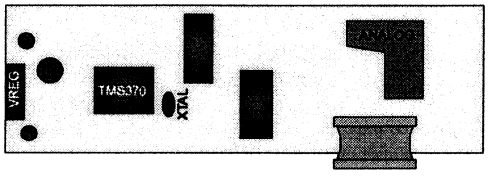
★ Place high-speed ICs close to power supply, with slower components located further away, and analog components even further still;

★ Place oscillator tank loops away from analog circuits, low-speed signals and connectors;

★ Build a gridded or solid ground between the IC, volt. reg and Vcc input, and tie the shield in at that point;

★ Locate the IC next to the volt. reg and the volt. reg next to where Vcc comes on the board;

★ Don't design in cable assemblies that fold over oscillators or high-speed devices.



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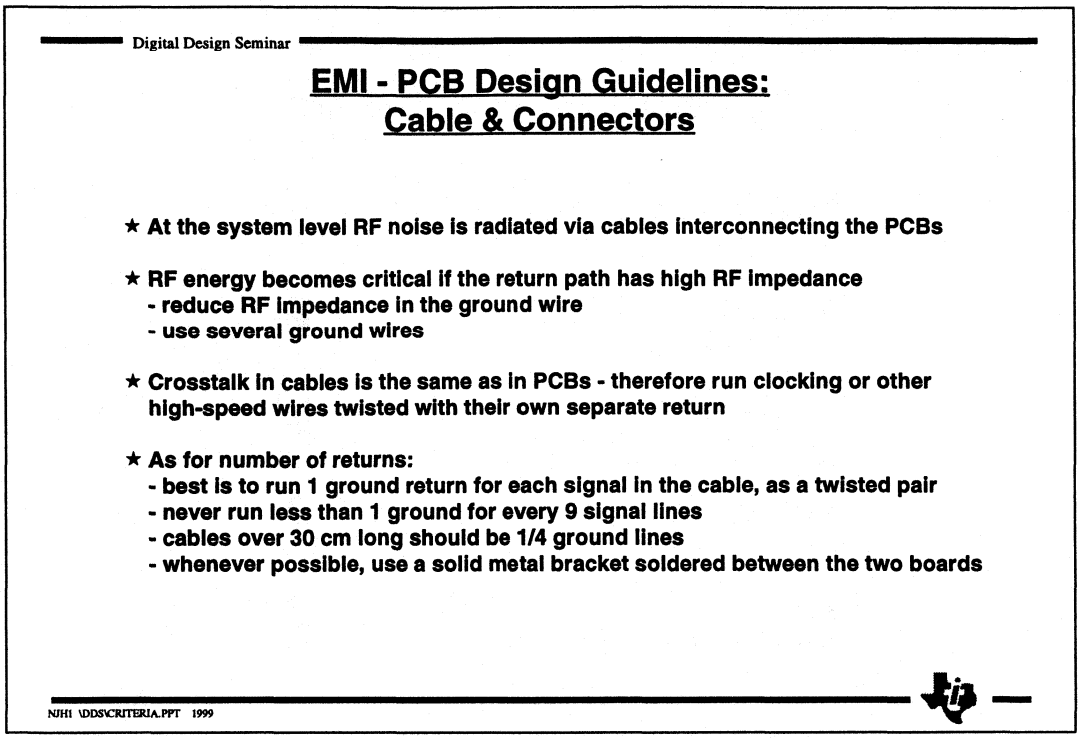
Board zoning (or floor-planning) a PCB is the first step towards designing EMC. Board zoning consists of creating zones on the PCB for analog, digital and noisy components and providing proper space for grounding. Also, devices should be arranged to minimize routing distances of EMI-critical signals, such as clocks, power, cabling and control signals.

High-speed ICs are placed close to the power supply, with slower components located further away, and analog components even further still. In this way the high-speed logic has less chance to pollute other signal traces.

Of special note, oscillator tank loops should be placed away from analog circuits, low speed signals and connectors.



The problem at the system level becomes the radiation due to cables interconnecting the PCB with any off-board support function, or other processor, display or keypad PCBs. Since there is usually only one ground wire between boards, this one inductive wire has to return all of the RF energy carried into the second PCB by the other (signal) wires.

If there is any impedance in the one ground wire (e.g. connector), a portion of the RF energy will not return to the IC's PCB via the ground wire, but rather through a radiated path. It will radiate off the second board and couple back to the first, but during that process that radiation can add noise in other locations in the system.

The key corrective action is to insure the conducted path for the return has a very low RF impedance. For low speed data transmission it is common practice to have at least 1 ground for every 9 signal lines in a cable or harness. The number is moving towards 1:5 with higher speeds. The best is to run 1 ground return for each signal line in a cable, as a twisted pair.

Whenever possible, there should be a solid metal bracket used as a mechanical brace, soldered between the two boards that serves both as a mounting bracket and as a robust RF ground return.

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System Design Criteria Summary

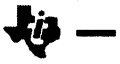
Switching Characteristics ☑
- *3.3V signal level have generally lower slew rate*

Slow Inputs Signals ☑
- *Use Schmitt Trigger inputs*

Crosstalk ☑
- *Use shielding line between signal traces*
- *Minimize output current wherever possible*

Decoupling ☑
- *Choose correct capacitor*

EMI ☑
- *Keep traces short and have good grounding*



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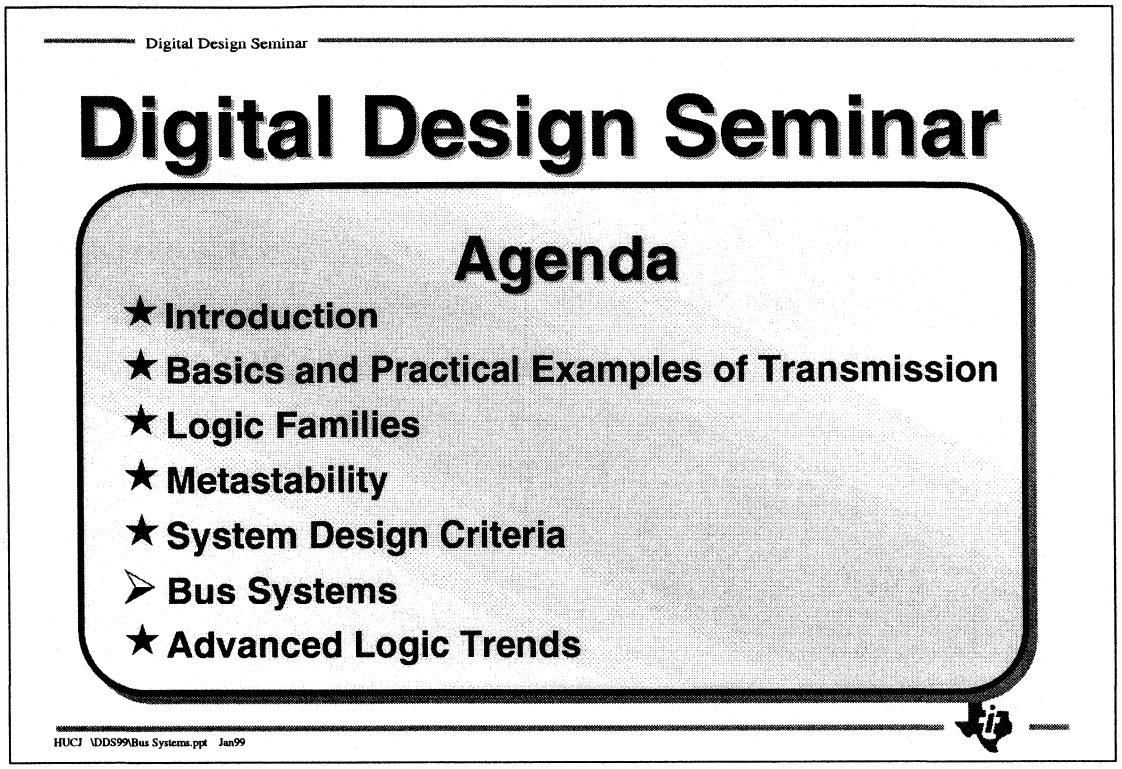
Digital Design Seminar
Digital Design Seminar
Agenda
★ Introduction
★ Basics and Practical Examples of Transmission
★ Logic Families
★ Metastability
★ System Design Criteria
➢ Bus Systems
★ Advanced Logic Trends
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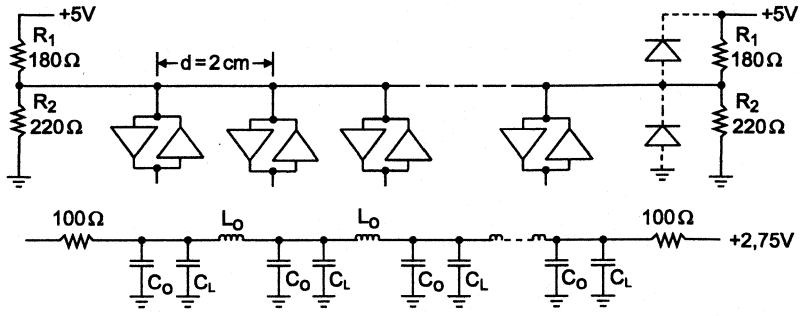
Digital Design Seminar

Bus Lines



Line parameter		
	unloaded	loaded with lumped capacitance
L_0	6 nH/cm	6 nH/cm
C_0	0.6 pF/cm	0.6 pF/cm
C_L	-	20 pF/2cm
Z	100 Ω	25 Ω
τ	6 ns/m	25 ns/m

Capacitance of the connector contact	≈ 5 pF
Capacitance of the printed wire	≈ 5 pF
Capacitance of the transceiver	≈ 10 pF
Lumped capacitance C_L	≈ 20 pF

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A signal line on a backplane bus compared to a signal line on a board is just the same wire with the same capacitive-layer (0.6pF/cm) and inductive layer (5nH/cm), the only difference being, that every 2 cm of the bus line there is additional capacitance from:

- a connector with a capacitance of 5pF
- a stub line on the plug-in-board (5pF) and
- the I/O-pin of a transceiver (10pF).

This 20pF additional capacitance, added every 2 cm, dramatically increases the capacitive layer from 0.6pF/cm to 20.6pF/cm. If we look at the basic equations

$$Z_0 = \sqrt{\frac{L'}{C'}}$$

$$\tau_0 = \sqrt{L' \times C'}$$

we can calculate an extreme decrease of the characteristic impedance from 100Ω to 25Ω and a massive increase of the signal propagation delay time from 6ns/m to 25ns/m.

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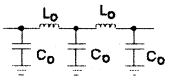
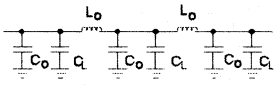
Transmission Line Parameter

		UNLOADED	LUMPED LOADING
			
INDUCTANCE	nH/cm	L_o	L_o
CAPACITANCE	pF/cm	C_o	$C_o + C_L$
LINE IMPEDANCE	Ω	$Z_o = \sqrt{\frac{L_o}{C_o}}$	$Z = \sqrt{\frac{L_o}{C_o + C_L}} = Z_o \sqrt{\frac{1}{1 + C_L/C_o}}$
PROPAGATION TIME	ns/m	$\tau_o = \sqrt{L_o C_o}$	$\tau = \sqrt{L_o(C_o + C_L)} = \tau_o \sqrt{1 + C_L/C_o}$
CUT OFF FREQUENCY	Hz	$\frac{1}{2\pi \sqrt{L_o C_o}}$	$F_o = \frac{1}{2\pi \sqrt{L_o(C_o + C_L)}}$

This table is an overview of the basic eqautions of transmission line theory. It compares unloaded signal traces and loaded bus-lines.

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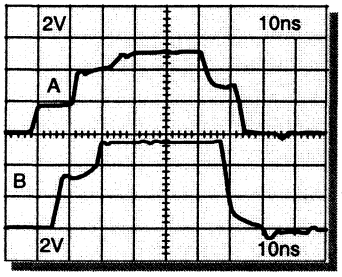
CMOS-Bus
SN74HCxxx



Bus driver SN74HC245

Z_O = 30 Ω; τ = 8 ns; L = 32 cm

Output impedance of the driver > Z_O

No line termination

A: Signal at driver output
B: Signal at line end

- ★ **No incident wave switching**
- ★ **Valid logic level after 2 x τ, in worst case only after 4 x τ**
- ★ **Due to the high output impedance of the driver no termination necessary**
- ★ **Not applicable with long bus lines**

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After a detailed look at the behaviour of bipolar outputs connected to a backplane-bus, we now look at CMOS outputs driving a backplane bus.

The low drive capability, and therefore high output impedance, (≈25Ω – 35Ω) of HCMOS devices and AHC devices makes it impossible to switch bus lines with the incident wave. Under worse case situations the signal settles after four times the propagation delay time of the signal on the bus line. For short buses and/or slow systems HC or AHC could be a acceptable solution.

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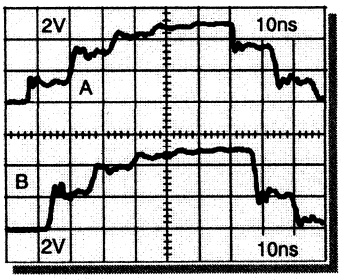
CMOS-Bus
SN74AHCxxx



Bus driver SN74AHC245

Z_O = 30 Ω; τ = 8 ns; L = 32 cm

Output impedance of the driver > Z_O

No line termination

A: Signal at driver output
B: Signal at line end

- ★ **No incident wave switching**
- ★ **Valid logic level after 2 x τ, in worst case only after 4 x τ**
- ★ **Due to the high output impedance of the driver no termination necessary**
- ★ **Not applicable with long bus lines**

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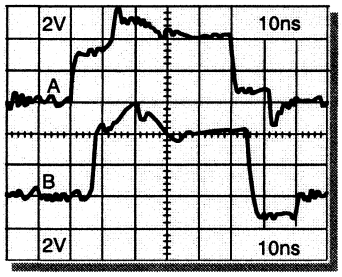
CMOS-Bus
SN74ACxxx



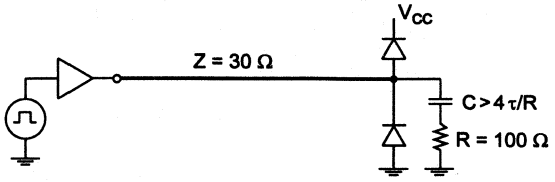
Bus driver 74AC245

Z_O = 30 Ω; τ = 8 ns; L = 32 cm

Output impedance of the driver > 10 Ω

Line termination R = 100 Ω and diodes

A: Signal at driver output
B: Signal at line end



★ **Low Signal distortion and low reflections due to line termination and clamping diodes**

★ **Incident wave switching capability sufficient for TTL compatible circuits**

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Advanced CMOS (SN74ACxxx) drivers have, with an output impedance of about 10Ω, the highest drive capability and lowest output impedance of all CMOS outputs. Because of this, incident wave switching is possible, especially for TTL compatible circuits (SN74ACTxxx). The high voltage swing of 5V and the low output impedance make the presence of line termination and clamping diodes necessary.

Advanced CMOS drivers generate a high current spike at the supply current because of the high voltage swing and the fast rise/fall times. These current spikes generate a lot of electromagnetic noise (EMC) and so Advanced CMOS is not the first choice in big backplane systems.

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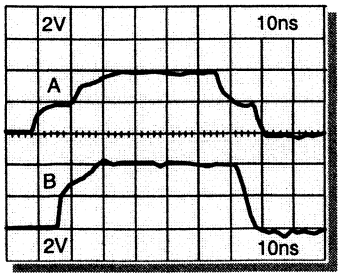
Line Driver SN74ALSxxx



Line driver SN74ALS245 (I_{OL} = 24mA
Z_O = 30 Ω; τ = 8 ns; L = 32 cm
No line termination
Output impedance of the driver ≈ Z_O
(impedance matching)

A: Signal at driver output
B: Signal at line end

- ★ **No incident wave switching**
- ★ **valid logic levels after 2 x τ**
- ★ **owing to matching of driver output impedance and line impedance, no undershoots**
- ★ **not applicable in fast systems with long bus lines**

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The output impedance of an SN74ALS245 pull-up transistor is in the range of 35Ω and is therefore higher than the impedance of the bus line (30Ω). The incident wave of the rising edge, which is calculated from the resistor divider, output impedance of the driver and line impedance, is therefore about

$$V_{Incident} = V_{OL} + \left(V_G \frac{30\Omega}{30\Omega + 35\Omega}\right) = 0.3V + (3.3V \times 0.46) = 1.8V$$

For the falling edge the situation is not much better. The pull-down transistor has a output impedance in the range of the line impedance and so the incident wave on the falling edge is again slightly below 2V.

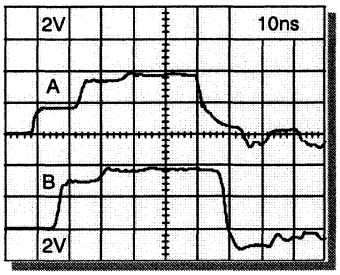
Because of this physical situation, valid logic levels on the bus-line are available after the reflected wave comes back from the end of the line (2 x τ).

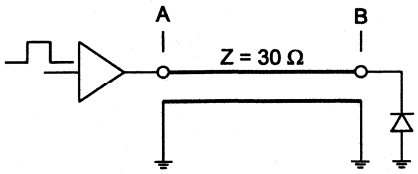
This type of bus-driver is not applicable for fast systems with long bus lines.

Digital Design Seminar

TTL-Bus

SN74ABT240, No Line Termination, only Clamping Diode





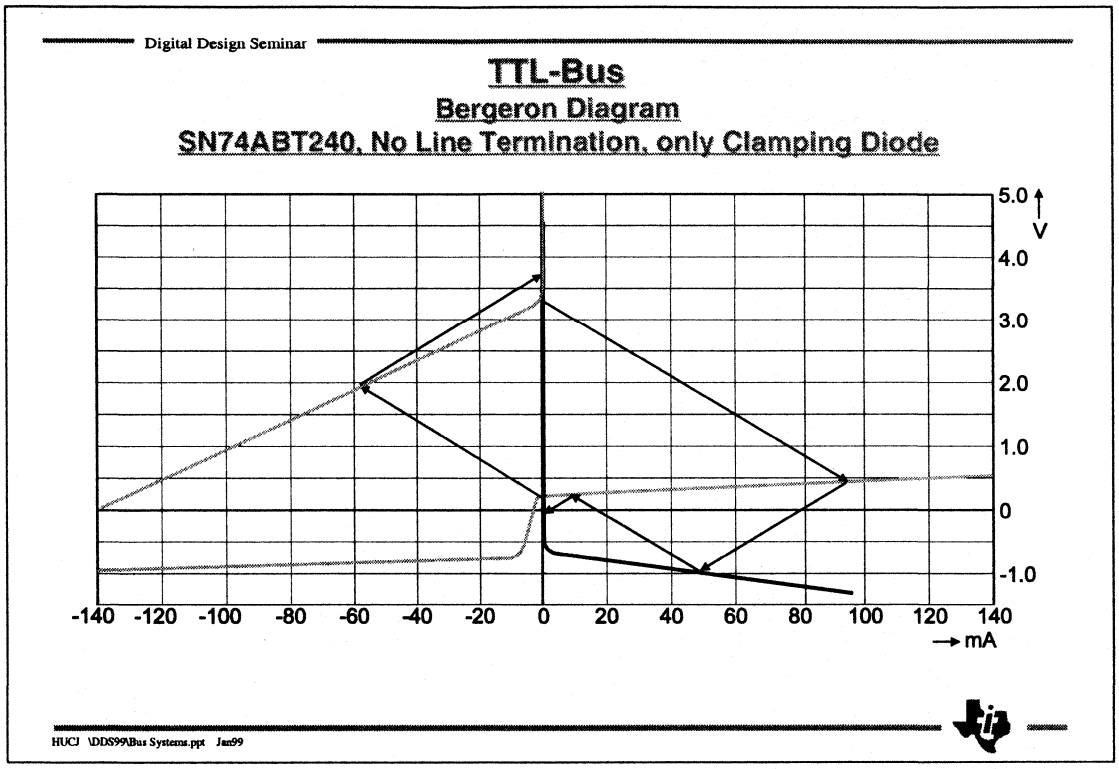
★ **The driver output reaches high level (>2 Volts) only after twice the propagation time**

★ **Negative undershoot at the line end is limited by the clamping diode**

If we take a driver of the latest BiCMOS technology for 5V supply voltage, the SN74ABT240, the output drive capability at the low level is higher than for the SN74ALS240 and hence the incident wave at the falling edge reaches a value of about 1V. But with the advantage of incident wave switching at the falling edge comes the disadvantage of a tremendous undershoot at the end of the signal line. In this situation we need at least a clamping diode at the line-end to limit the undershoot to about -0.7V.

The higher output impedance of the pull-up transistor still generates a incident wave below 2V at the rising edge and thus incident wave switching is not possible here.

For a fast system with a long bus this modern technology still is not able to switch all slopes with the incident wave.



The Bergeron Diagram shows the behaviour of an SN74ABT240 which is driving a transmission line of 30Ω with a clamping diode at the end of the transmission line. A comparison between the measurement on the page before and the theoretical contruction here shows good correspondence.

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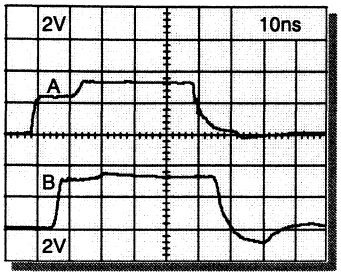
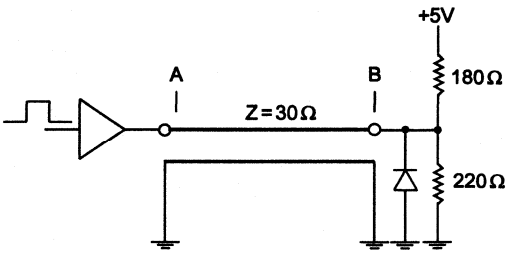
TTL-Bus

SN74ABT240, Line Termination with Thevenin Network





★ **Incident positive wave has an amplitude >2 Volts**

★ **Line reflections are sufficiently dampened by a 100 Ω termination**

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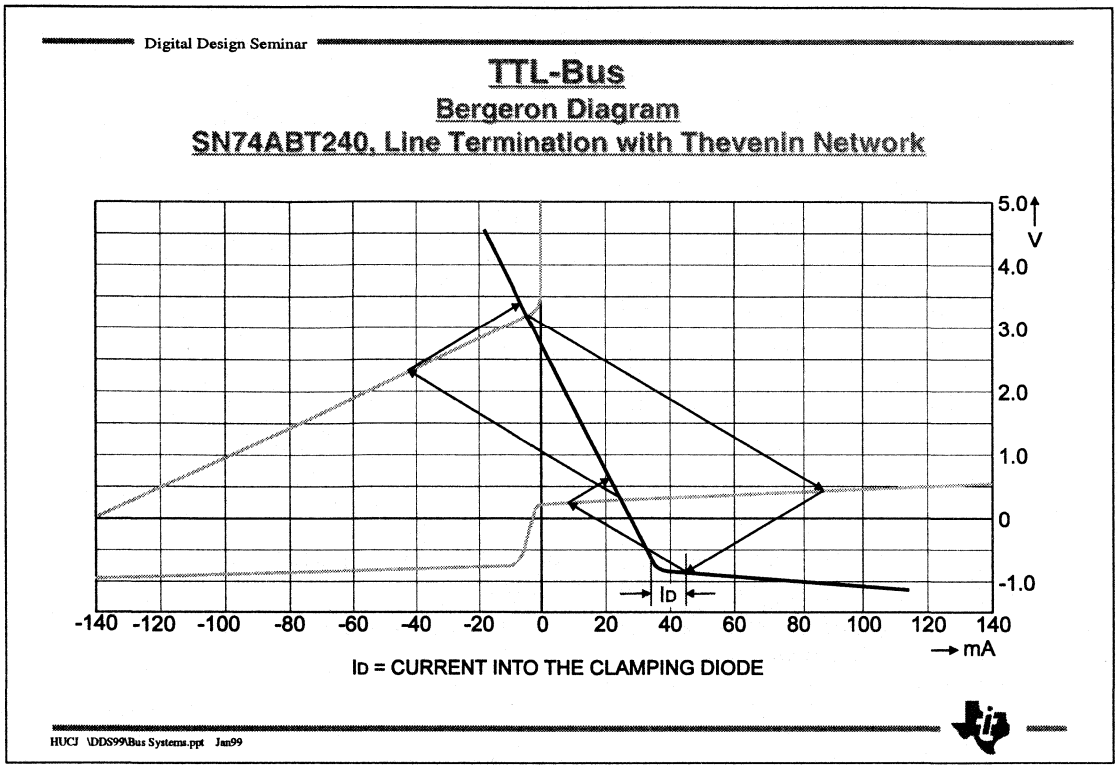
An additional Thevenin termination network of 180Ω to Vcc and 220Ω to GND at the end of the transmission line reduces the output impedance of the pull-up driver (a combination of the ABT240 and termination network) and thus helps at the rising edge. This lifts the incident wave of the rising edge above the 2V hurdle and now we are able to switch the rising and falling edge with the incident wave.



The Bergeron Diagram shows the behaviour of an SN74ABT240 driving a transmission line of 30Ω with a Thevenin termination network of 180Ω to Vcc and 220Ω to GND and a clamping diode at the end of the transmission line. A comparison between the measurement on the page before and the theoretical construction here shows good correspondence.

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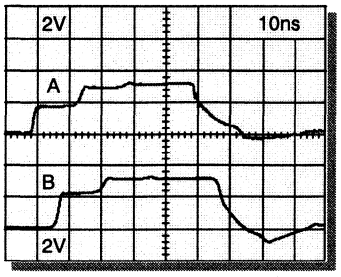
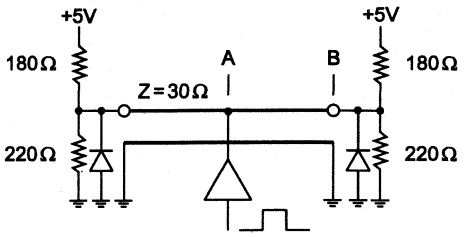
TTL-Bus

SN74ABT240, Driver in the Middle of the Bus, Thevenin Termination





★ **Effective load = 15 Ω**

★ **Driver output reaches high level only after the reflected wave is returned from the line end**

★ **Line reflections are dampened sufficiently by the termination network**

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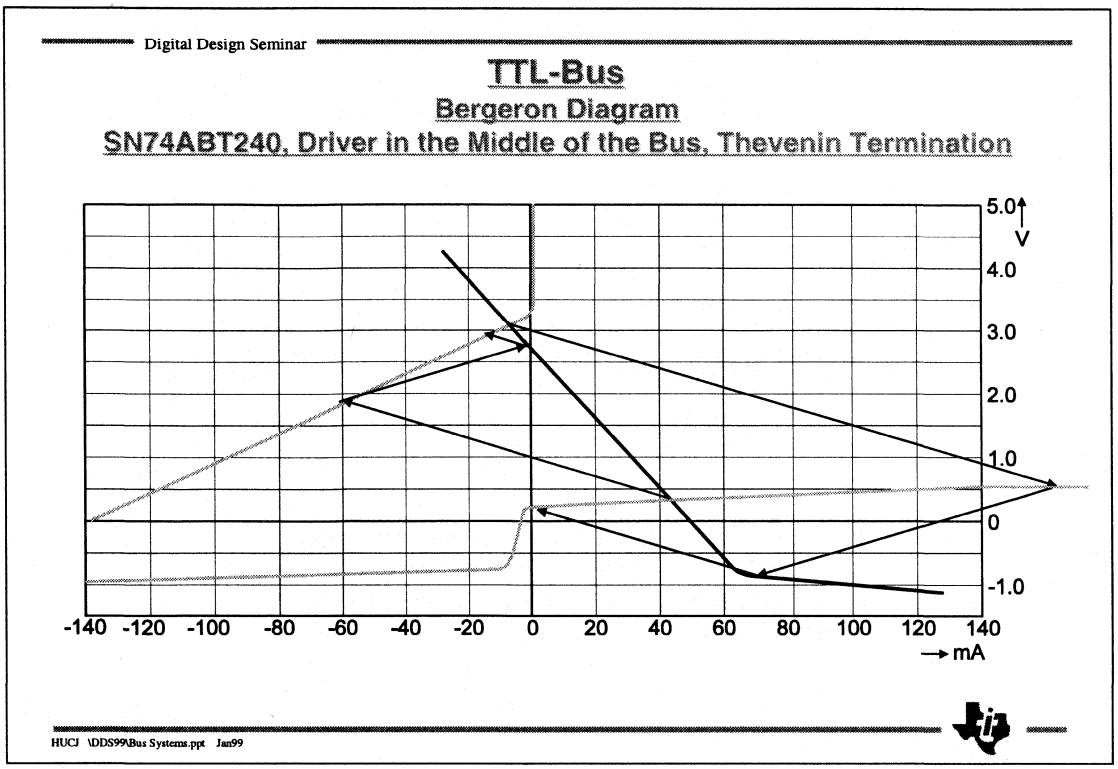
In the examples on the previous pages the bus-driver had to drive a transmission line with a impedance of 30Ω. But in real bus application only two drivers sit at the ends of the signal line and most of the bus-drivers are located in the middle of line. These drivers in the middle of the line now have to drive a 30Ω line to the left and a 30Ω line to the right with an overall impedance of 30Ω || 30Ω = 15Ω.

Although we are using Thevenin termination networks and clamping diodes on both ends of the signal line, in this situation the SN74ABT240 is not able the switch the bus-level with the incident wave from low to high or vice versa. The output impedance of the driver is too high to generate a reasonable output voltage. For the calculation we need the resistor divider of the driver's output-impedance R_G and line impedance Z_0:

$$V_{Incident} = V_G \frac{Z_0}{Z_0 + R_G}$$



This Bergeron Diagram shows the behaviour of an SN74ABT240 driving two transmission lines of 30Ω equivalent to one 15Ω-line with a Thevenin termination network of 180Ω to V_{CC} and 220Ω to GND, and a clamping diode at both ends of the transmission line. A comparison between the measurement on the page before and the theoretical construction here shows good correspondence.

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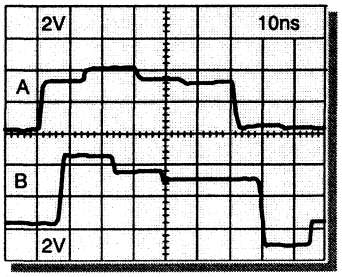
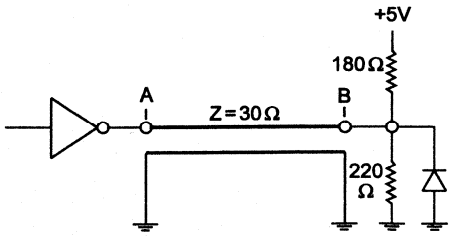
TTL-Bus

'IWS'-Line Driver SN74ABTH25xxx

IWS Driver, Thevenin Termination





★ **IWS (= Incident Wave Switching) drivers have a greatly improved drive capability in the high state**

★ **High level at the driver output is achieved with the incident wave**

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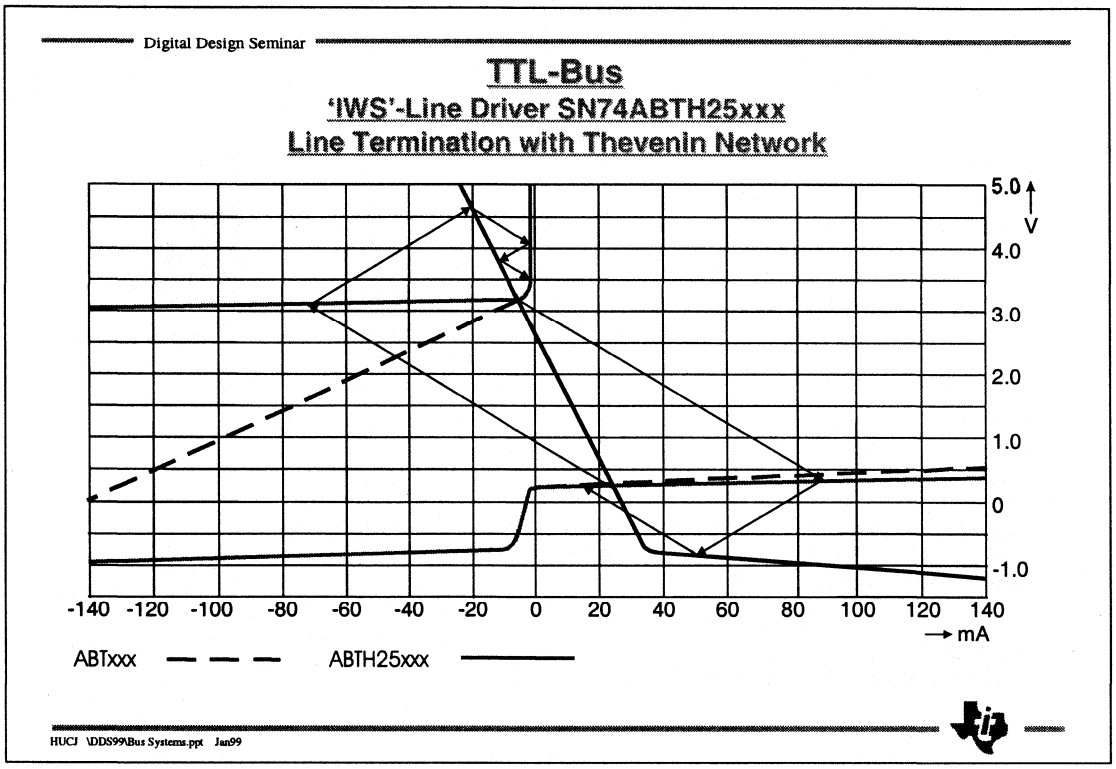
The main reason for the low amplitude of the incident waves is the impedance of the driver-output which is too high compared with the low impedance (30Ω) of a bus-line. Often a driver is sitting in the middle of a bus and has to drive two 30Ω lines in parallel. As a result of this physical situation we need a driver with an extremely low output impedance to be able to switch a bus line with the incident wave.

The Texas Instrument IWS drives family (SN74ABTH25xxx) has a guaranteed high level DC output current I_{OH} = -80mA and low level DC output current I_{OL} = 188mA. This is possible only because the output impedance for low and high level is below 2Ω. Such a low impedance driver easily generates incident waves above 3.3V at the rising edge and below 0.5V at the falling edge when driving a 30Ω line. If the load is 15Ω, it still reaches more that 3.2V and less than 0.6V with the incident wave.

The SN74ABTH25xxx IWS-line drivers are the ideal solution for fast TTL-compatible systems with long bus-lines.



Here the Bergeron Diagram shows the behaviour of an SN74ABTH25240 IWS-line-driver driving a transmission line of 30Ω with a Thevenin termination network of 180Ω to Vcc and 220Ω to GND and a clamping diode at the end of the transmission line. A comparison between the measurement on the page before and the theoretical construction here shows good correspondence.

Digital Design Seminar

Enhanced Transceiver Logic - ETL

Benefits:

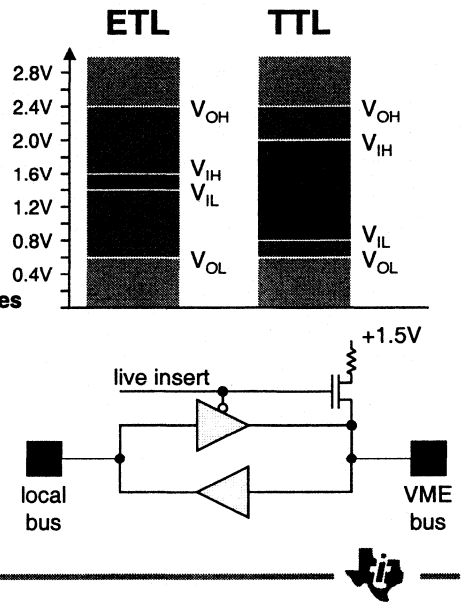
- ★Extends life of TTL characteristic bus
- ★Enhanced noise margin
- ★Supports live insertion
- ★Lower part-to-part skew
- ★Higher driver capability

Characteristics:

- ★Tighter input threshold (1.4 ... 1.6 V)
- ★Input circuit is current mode switch (compensates for temperature, voltage, process)
- ★Precharge function (to 1.5 V) added to minimize capacitive discharge to active backplane
- ★VCC-BIAS used to control high impedance state during live insertion

Products:

SN74ABTE16245, SN74ABTE16246



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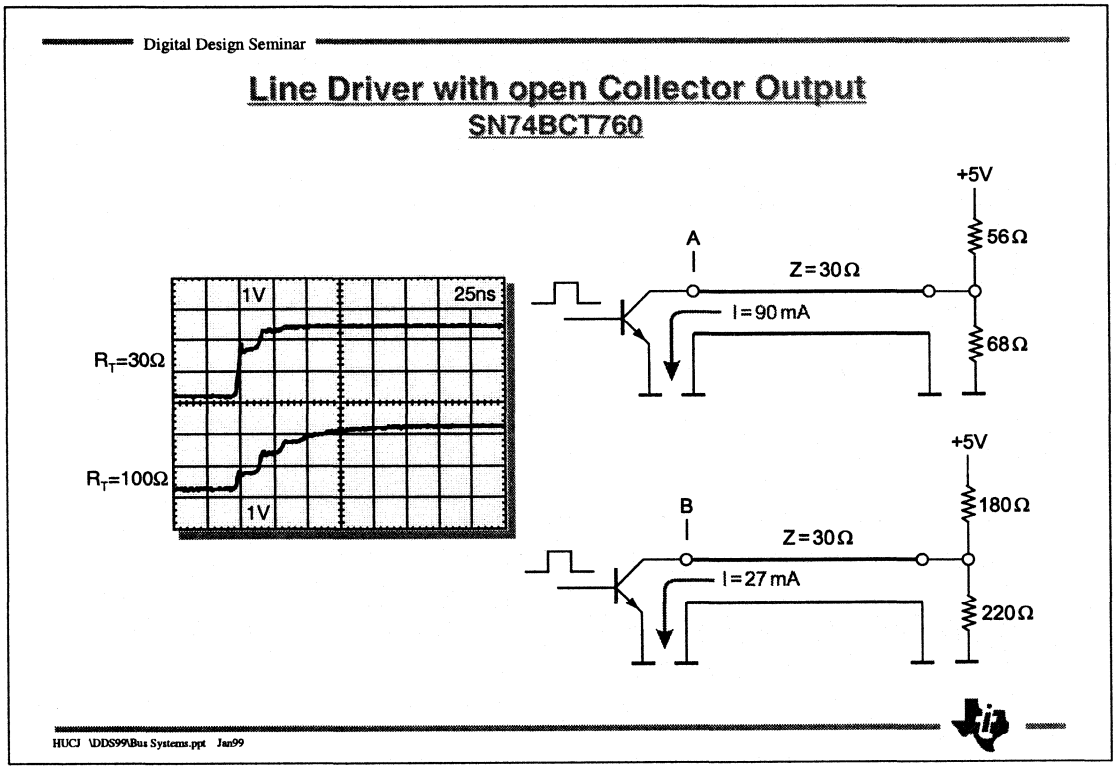
To increase the speed of the VME-bus the new VME-64 has been defined. The physical layer of VME-64 is called the Enhanced Transceiver Logic (ETL).

Here the standardization committee has found another way to speed up the bus system and still keep backwards compatibility with the older TTL-compatible VME-bus. With differential amplifiers at the inputs, the threshold (1.5V) is better defined than with the common TTL-inputs and so V_{IL} can be defined to be below 1.4V (TTL: $V_{IL} < 0.8V$) and V_{OH} above 1.6V (TTL: $V_{OH} > 2V$). With this modification we gain room for the incident waves at the inputs which now have to jump above 1.6V instead of 2V and below 1.4V instead of 0.8V for standard TTL devices.

The specification also includes the precharge feature for live insertion. Each pin has an overall capacitance of about 20pF. If a card is inserted while the system is running, the precharge feature charges the 20pF capacitance of each signal-pin to the threshold (1.5V) before the pins are connected to the bus-lines. This makes sure that the voltage spike, which is generated by changing the capacitance of the pins to a valid logic high or low level, never exceeds the threshold.

TI's offers SN74ABTE16245 and SN74ABTE16246 as bus transceivers to the ETL specification.

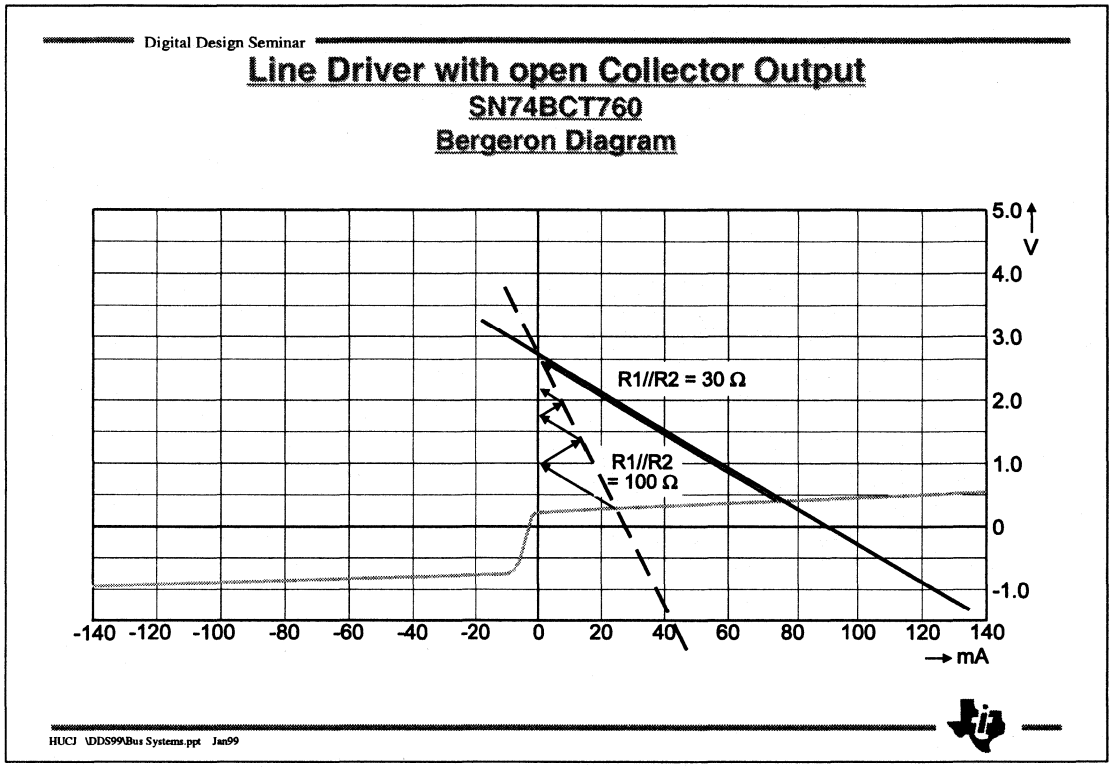


Always some bus-signals are carried out in open collector or open drain mode. In these cases, the falling edge is actively generated by the driver, what we learned previously about TTL drivers on bus systems is also valid here: Only a low impedance driver can switch the bus with the incident wave.

The rising edge is generated by the passive pull-up-network. If we choose a pull-up-network with a output impedance like the impedance of the bus-line, then we see a excellent rising edge at the driver output with the disadvantage of a tremendous low-level-current of 90mA for one signal-trace.

Because this current is not acceptable we change the output impedance of the pull-up-network to about 100Ω. Now for the rising edge, a driver with 100Ω tries to pull-up a transmission line of 30Ω with the result that we have to wait for several reflections of the bus-signal until we reach a valid logic high level.

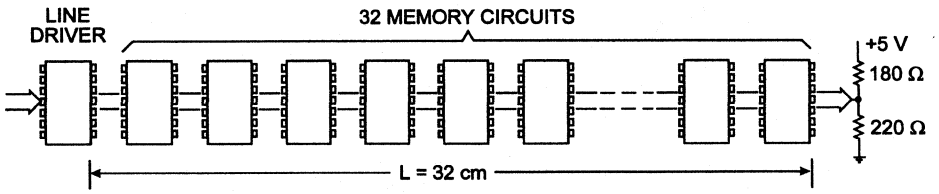
Remember: Rising edges on open-collector bus-lines are always slow ... and there is no generally valid work around.



This Bergeron Diagram shows the behaviour of the rising edge of a open collector bus-line. A pull-up-network with an impedance of 100Ω compared with a 30Ω network drives a transmission line of 30Ω. A comparison between the measurement on the page before and the theoretical construction here shows good correspondence.

Digital Design Seminar

Memory System with 1 M Words at 32 Bits
Version 1



- ★ **Resulting line impedance = 30 Ω**
- ★ **Line driver with I_{OL} = 64 mA required (AS, F, BCT, ABT, LVT)**
- ★ **High power dissipation in the termination network and high component count**
- ★ **Signal propagation time = 7 ns / 32 cm**
  ⇒ additional propagation delay time = 14 ns

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Besides huge backplane busses there are also smaller busses in computer systems: e.g. a memory bus on a processor board. These memory busses add, for each 1 cm length, the capacitance of one I/O pin (10pF) to the capacitive layer of the signal trace. So the capacitive layer changes from 0.6pF/cm to 10.6pF/cm, exactly the same value we see on backplane busses with 20pF connected each 2cm. As a result the impedance of the signal trace is about 30Ω and the propagation delay time of the trace about 20ns/m.

In the example above, 32 memory chips are placed in one row and this leads to a line length of about 32cm and a signal delay time of 7ns along the bus-line. When a memory read takes place we have to add two times the propagation delay time of the trace (2 * 7ns = 14ns) to the RAM access time. This additional delay time comes only from the wire on the boards, and not from the delay time of active electronics like the bus transceiver.

Because of the 7ns delay on the signal line is longer than the rise-/fall-time of the signal, the designer has to terminate the line in parallel to avoid signal reflection, which would increase the settling time of the signal on the trace beyond the delay time of 7ns. DC-current through the termination network is the result.

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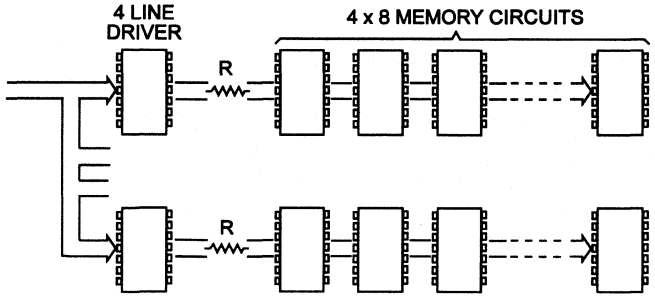
Memory System with 1 M Words at 32 Bits
Version 2



★ **Resulting line impedance = 30 Ω**

★ **Signal propagation time 1.75 ns / 8 cm (20 ns/m), therefore total propagation time 3.5 ns only**

★ **Matching of driver impedance by series resistors (R = 10 ... 20 Ω),**
⇒ no increased power consumption!
(line driver with I_{OL} = 24 mA sufficient ⇒ LS, ALS)
Line driver with integrated series resistor available, e.g. SN74ABT2240, SN74ABT5400A

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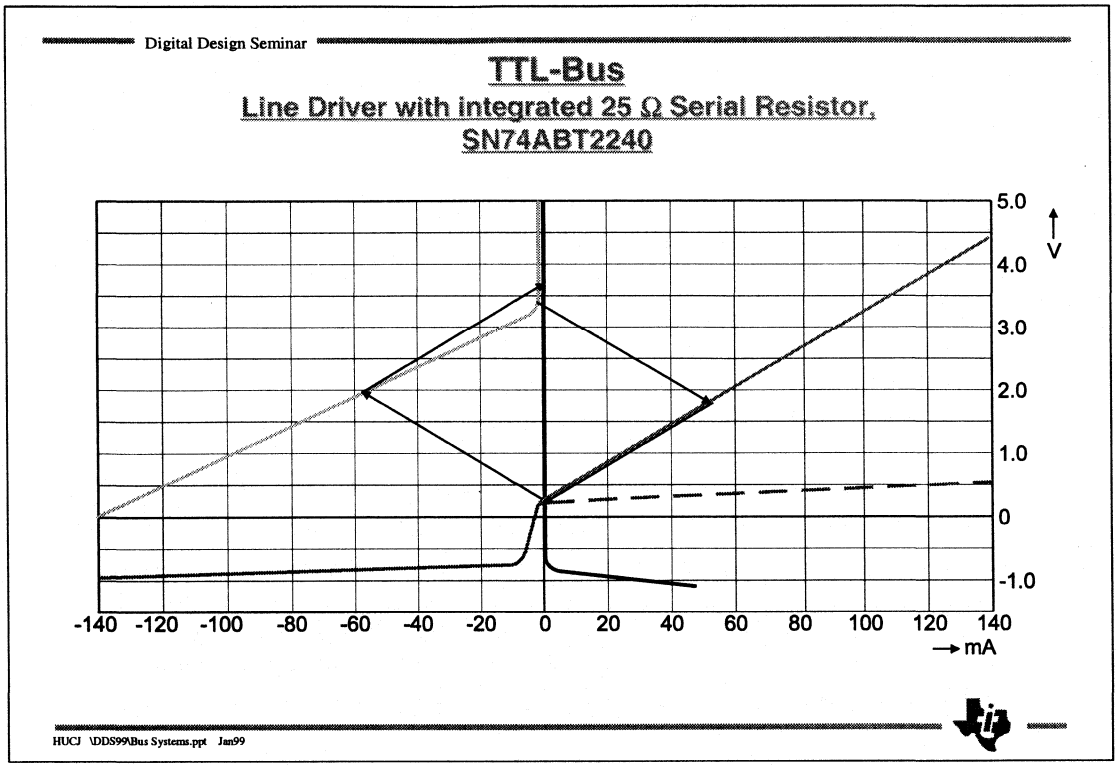
Here the design of the previous page has been modified to speed up the RAM access. Now the 32 RAM chips are located in 4 rows of 8 memory devices. In this case the length of the bus trace is only 8 cm, and the propagation delay time along this line is 1.75ns.

The calculation of the access time shows now 3.5ns for the wire, which has to added to the RAM access time. With 3.5ns compared to 14ns of the previous example, the RAM access has been improved by more that 10ns. Now the designer can choose RAMs with a access time which are 10ns slower. The cost of cheaper RAM circuits more than offsets the increased cost of four instead of one bus-transceiver.

Now twice the signal delay time (3.5ns) is in the range of the rise/fall time of a typical digital signal and hence parallel termination is no longer necessary. Serial termination has been selected to avoid undershoots that could lead to malfunction of the RAM circuits.



This Bergeron Diagram shows the behaviour of the rising and falling edge of a memory driver circuit with an output impedance of 30Ω driving a memory-bus line with an impedance of 30Ω. A comparison between the measurement on the page before and the theoretical construction here shows good correspondence.

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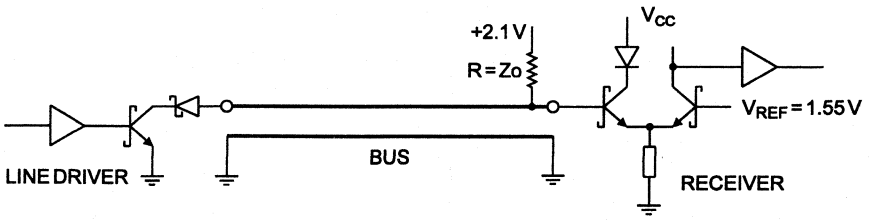
Backplane Transceiver Logic - BTL



★ **Reduced voltage swing: V_L = 1V; V_H = 2.1 V**

★ **High drive capability: I_{OLmax} = 100 mA ⇒ Incident wave switching down to 10Ω or 2 || 20Ω line impedance**

★ **Correct line termination by a pull-up resistor at the line end avoids line reflections**

★ **Decoupling diode reduces output capacitance to < 5 pF ⇒ increased line impedance**

★ **Maximum output edge rate 2 ns ⇒ Trapezoidal wave-form reduces system noise**

★ **Supports live insertion/withdrawal ⇒ Output high impedance when V_{CC}=0V**
⇒ Power-up 3-state control at outputs
⇒ BIAS V_{CC} pin to pre-charge BTL outputs

★ **Differential amplifier guarantees stable threshold voltage of the receiver**

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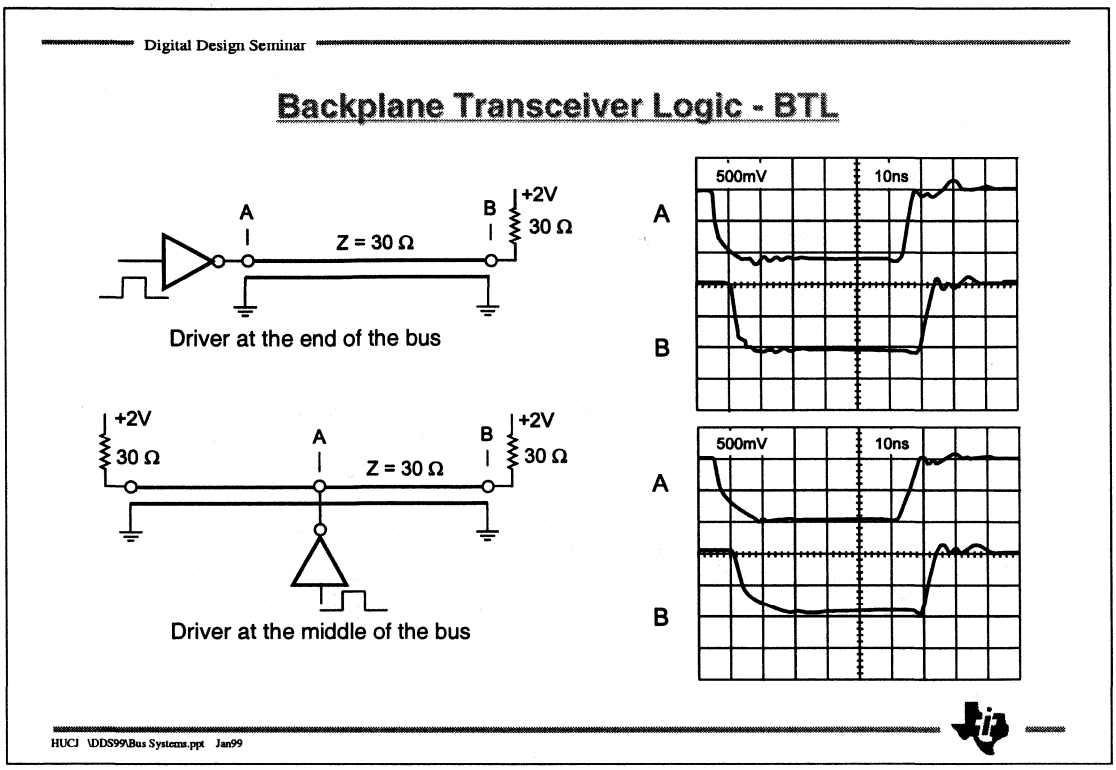
One of the problems of TTL or CMOS circuits driving bus lines comes from the high voltage swing: Correct termination is not possible and big I_{CC} current spikes are necessary to enable incident wave switching. A bus system with reduced voltage swing could solve a lot of problems.

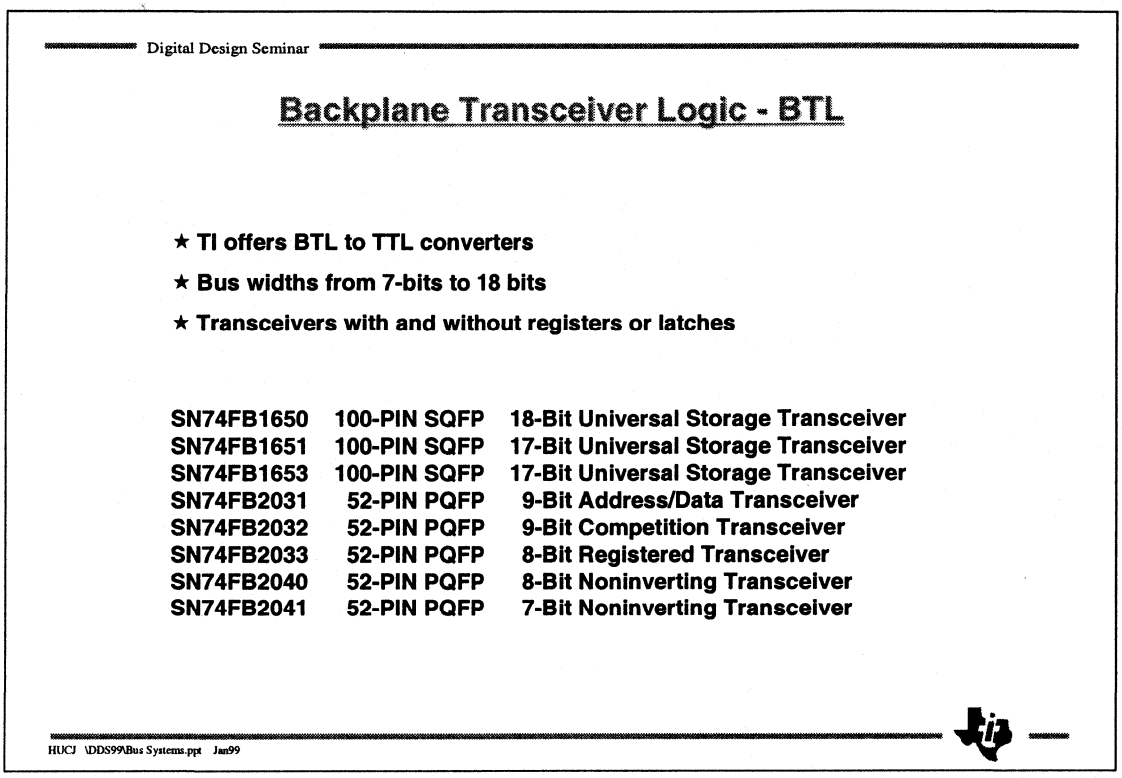
The physical layer of the Future-Bus is called Backplane Transceiver Logic (BTL) and works with a voltage swing of 1.1V only. The bus system is open collector. The low level of 1V is generated by the saturation voltage of the pull-down transistor and the forward voltage of the serially connected diode. The high level of 2.1V comes from the termination resistor connected to a termination voltage of 2.1V. The value of the termination resistor is equal to the impedance of the bus-line and therefore the bus-line is terminated correctly. For safe detection of the logic levels, the inputs are designed with differential amplifiers and a threshold at 1.55V, exactly in the middle of the voltage swing.

To reduce I_{CC} current spikes, the fall-time is defined to be at least 2ns. The rise time is not generated by active electronics, but by the pull-up resistor.

All necessary features for live insertion and withdrawal have been included: The outputs are in high impedance when V_{CC}=0V and during power up/down (Power-up 3-state). The pre-charge feature reduces voltage spikes when the I/O connects to the bus line (see ETL logic).



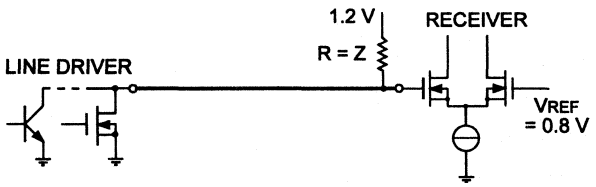
Measurements of BTL circuits driving 30Ω bus-lines show excellent wave forms. In the upper example a BTL output drives a point-to-point connection with a characteristic impedance of 30Ω and a termination resistor of 30Ω at the end of the line. In the second example the BTL driver is sitting in the middle of the bus-line, driving two signal traces of 30Ω. Both lines are correctly parallel terminated with 30Ω pull-up resistors.

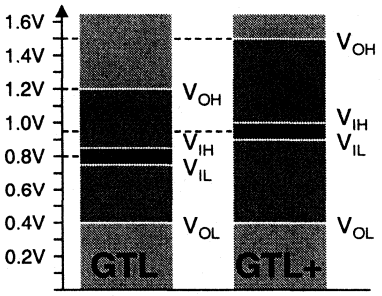


All the circuits TI offers are bi-directional BTL to TTL converters. The designer can choose from 7- to 18-bit bus width and gets bus functions with and without registers and/or transparent latches.

Digital Design Seminar

Gunning Transceiver Logic - GTL / GTL+





★ **Reduced voltage swing: GTL: V_L = 0.4V; V_H = 1.2 V;**
GTL+: V_L = 0.4V; V_H = 1.5V

★ **Low drive capability: I_{OLmax} = 40 mA**
⇒ Incident wave switching down to 20Ω or 2 || 40Ω line impedance
⇒ Low power dissipation (0.4V x 40mA per output)

★ **Correct line termination by a pull-up resistor at the line end avoids line reflections**

★ **High data rates (> 100 MBit/s)**

★ **Integration of line driver and receiver into ASICs possible**

★ **Doesn't support live insertion/withdrawal ⇒ Output high impedance when V_{CC}=0V**

★ **Differential amplifier guarantees stable threshold voltage of the receiver**

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The basic concept of a GTL bus is very similar to a BTL system.

Because of the missing diode in the open collector/drain outputs the low level is 0.4V. With a chosen high level of 1.2V the voltage swing is reduced to 0.8V only. Again the threshold is in the middle of the voltage swing at 0.8V.

The drive capability of GTL outputs is defined to be 40mA, which enables a output to drive one termination resistor of 0.8V / 40mA = 20Ω. If the bus line is terminated correctly, the lowest impedance that can be driven by a GTL driver in the middle of a bus now is 40Ω (in both directions: 40Ω || 40Ω = 20Ω).

On the previous pages, the heavily loaded backplane bus always had a line impedance of 25Ω to 30Ω. Here we see that a 40Ω bus is not heavily loaded and GTL was designed for a smaller bus on a board, e.g. between a processor and its memory. Because the target application for GTL is not a backplane bus, but a bus on a board, no requirements for live insertion/withdrawal have been included into the specification.

As a result of the 0.8V swing and the 40mA I_{OL} the maximum power dissipation of one output is 16mW. It is thus possible to integrate these low power drivers into ASICs.

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Gunning Transceiver Logic - GTL / GTL+

★ TI offers GTL and GTL/GTL+ to TTL converters

★ Bus width from 7 bits to 18 bits

★ Transceivers with and without registers or latches

Released:		
SN74GTL16612	**56-PIN SSOP/TSSOP**	**18-Bit Universal Storage Transceiver**
SN74GTL16616	**56-PIN SSOP/TSSOP**	**17-Bit Universal Storage Transceiver with buffered clock output**
SN74GTL16622A	**64-PIN TSSOP**	**18-Bit GTL/GTL+ Registered Transceiver**
SN74GTL16923	**64-PIN TSSOP**	**18-Bit LVTTL TO GTL/GTL+ Bus Transceiver**
Planned:		
SN74GTL16922	**64-PIN TSSOP**	**18-Bit GTL/GTL+ Registered Transceiver accepts TTL-compatible CMOS signals (0V/5V) at TTL inputs.**

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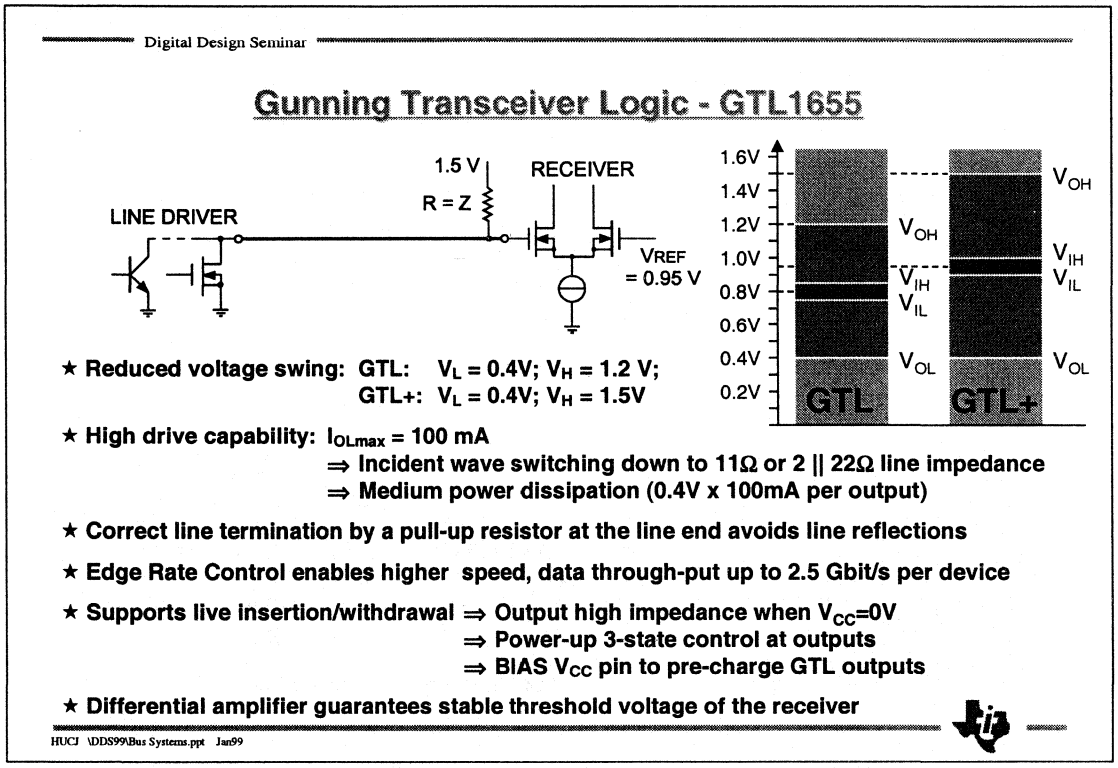
All the circuits TI offers are bi-directional GTL to TTL converters. The designer can choose between 17- and 18-bit bus-width and select bus functions with and without registers and/or transparent latches. The SN74GTL16616 also includes a separate buffered path for the clock signal.



With the SN74GTL1655 the benefits of the BTL family and GTL family have been combined within one device.

The drive capability of the SN74GTL1655 outputs has been enlarged to 100mA, which enables a output to drive one termination resistor of 11 Ohms.

$$R_T = 1.1V / 100mA = 11\Omega.$$

If the bus line is terminated correctly, the lowest impedance that can be driven by a GTL driver in the middle of a bus now is 11Ω (22Ω || 22Ω).. Considering both directions the value for the termination resistors is in this case 22Ω .

With the GTL1655 even the heavily loaded backplane bus which has a line impedance of 22 Ω to 30Ω easily can be served.

All the features for live insertion and withdrawal have also been included in the GTL1655: The outputs are in high impedance when V_{CC}=0V and during power up/down (Power-up 3-state); and the pre-charge feature reduces voltage spikes when the I/O connects to the bus line (see also ETL logic).

The SN74GTL1655 posses selectable edge rate control (ERC) for variable rise and fall rates so that the designers can fine tune their circuits for maximum data through put as system loading dynamically changes. The edge rate control minimizes bus settling time.

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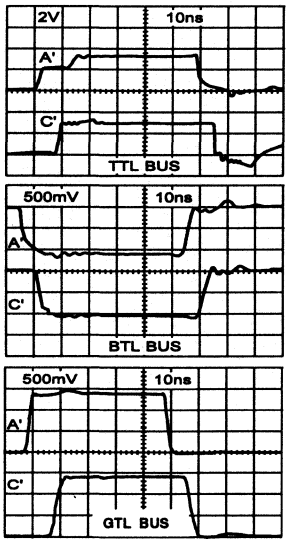
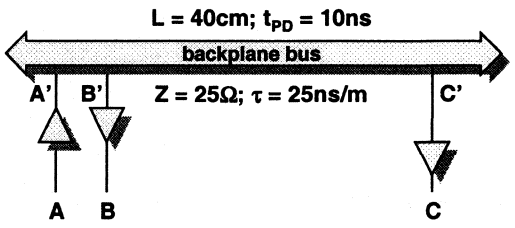
Speed Comparison of Circuit Concepts





		t_{PD}	Total propagation time A > B	A > C
ABT	SN74ABT245	4.6 ns	29.2 ns*)	19.2 ns
IWS	SN74ABT25245	4.3 ns	8.6 ns	18.6 ns
BTL	SN74FB2031	5.0 ns	10.0 ns	20.0 ns
GTL	SN74GTL1655	4.3 ns	8.6 ns	18.6 ns

* Settling time = 2 x propagation time

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As a summary of the bus system section a comparison between three bus concepts is shown. To find out the bus speed, an investigation of the propagation delay times from input A to the outputs B and C is done:

Example 1:
ABT circuits are quite fast buffers with a max. propagation delay time of 4.6ns only. Because they are not able to switch a bus signal with the incident wave, we have to wait until the reflected wave travels back to the input B'. Now the overall max. delay time from input A to output B is 29.2ns.

Example 2:
The usage of the SN74ABT25245 IWS (Incident Wave Switching) driver enables incident wave switching. Here the propagation delay time from input A to output B is 8.6ns only and the speed limiting path is now from input A to output C with 18.6ns - still more than 10ns faster than example 1 with SN74ABT245.

Example 3:
On a backplane bus, BTL drivers show about the same speed as IWS drivers. With correct parallel line termination and the reduced voltage swing we get excellent waveforms combined with very low noise.

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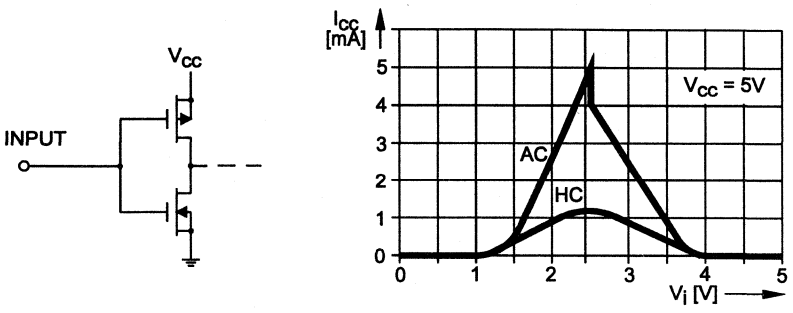
Supply Current at Floating CMOS-Inputs



When the input voltage of a CMOS circuit is between the defined voltage levels (low or high) -e.g. floating-, the P- and N-Channel transistors conduct simultaneously. This results in increased supply current.

Besides the different bus concepts there are some problems that can be seen on most bus systems. One of these problems is a floating bus line which leads to an open input.

The diagram above shows an input of any standard CMOS or BiCMOS circuit. Normally this input sees only 0V (low) or 5V (high) and in this case one of the two transistors is ON and one is OFF. Hence nearly no supply current is flowing from V_{CC} to GND.

If CMOS inputs are connected to a floating bus line, any voltage between V_{CC} and GND can be observed. With the input voltage close to the threshold value, both transistors are partly switched ON and now supply current (I_{CC}) can flow from V_{CC} to GND.

The graphic shows this behaviour of HC and AC circuits: With an input voltage of 2.5V the supply current of a HC circuit can rise more than 1mA per input. Looking at a 32-bit bus with 10 modules the increase of I_{CC} here can be 32 x 10 x 1mA = 320mA! Using Advanced CMOS (AC) circuits will result in a 5 times higher current, in this example 5 x 320mA = 1.6A.

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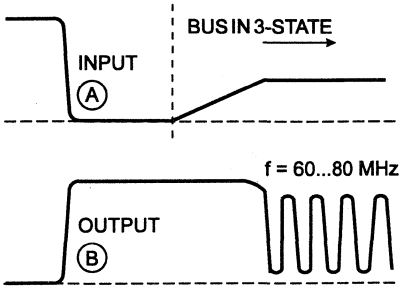
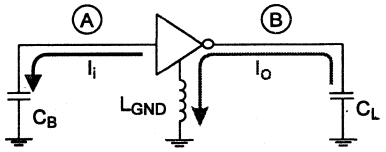
Oscillation on a Floating Bus Line





$$\frac{\Delta v}{\Delta t} = \frac{\Sigma I_i}{C_B} \approx \frac{500\,\mu A}{500\,pF} = 1\,V/\mu s$$

★ **When a bus line is left floating, the line is charged by the input currents of the receivers attached to the bus up to the threshold voltage.**

★ **The feedback via the GND inductance L_{GND} causes an oscillation. The resulting output stage currents I_O of these circuits overload and destroy the devices.**

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Another effect that can be seen on floating bus lines is device oscillation:

When a bus line is left floating, it is charged by the leakage currents of all receiver inputs attached to the bus line (e.g. from L to H). When this leakage current charges the bus line above the threshold voltage, the output of the driver switches (e.g. from H to L). For this transition of the output a current spike is necessary and via the VCC and GND inductance L_{GND} the internal reference for the threshold voltage drifts away. The input voltage does not change, but the threshold changes and so the input of the driver reads a change in the logic input-level (e.g. back from H to L). Thus the output switches again (e.g. from L to H).

Under worse case conditions this behaviour can lead to a high frequency oscillation. The output stage currents I_O of the circuits involved overload the circuit and destroy the devices.

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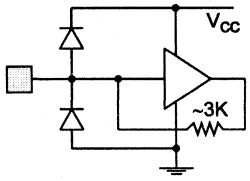
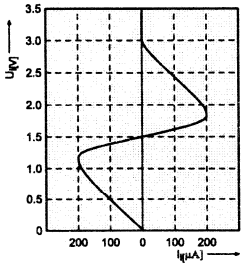
Bus Holders SN74ACT107x



- ★ **Bus holders ensure valid logic levels in CMOS bus systems, when all drivers are inactive (3-state).**
- ★ **No pull-up resistors are required!**
- ★ **Integrated clamping diodes limit the under- and overshoots caused by line reflections and thus ensure system integrity.**



Type	Function	Package
SN74ACT1071	10-Bit Bus Holder	16 Pin SOIC/SSOP
SN74ACT1073	16-Bit Bus Holder	20 Pin SOIC/SSOP

SN74ABTHxxx, SN74LVTHxxx, SN74ALVCHxxxx, SN74LVCHxxx

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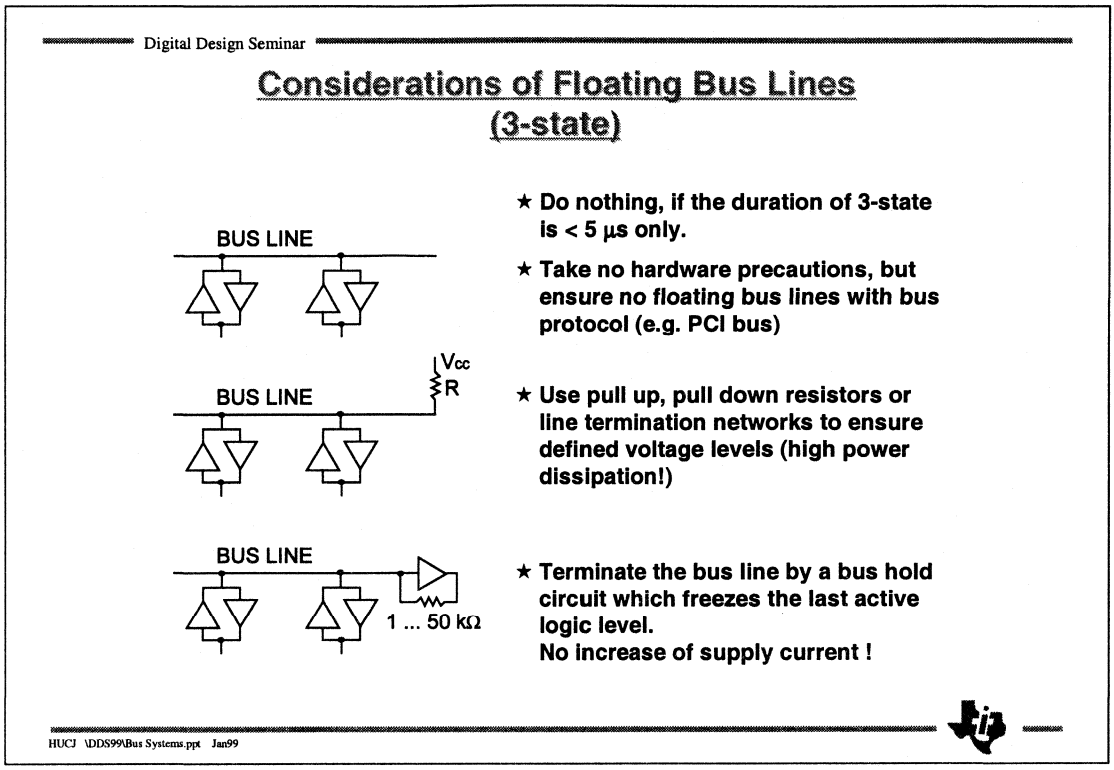
To address the problem of floating bus lines and open inputs, TI made many investigations and looked at various solutions to ease the design of bus systems.

One solution for floating bus lines is the Bus Hold circuit. This circuit holds the last valid logic level during the high impedance state and the floating bus line is held at a valid logic level. No other precautions have to be taken to avoid problems that arise from floating bus lines.

Bus hold circuits are included in the inputs of SN74ABTHxxx, SN74LVTHxxx, SN74ALVCHxxx and SN74LVCHxxx circuits. Ten or sixteen Bus-Hold circuits with integrated clamping diodes to V_{CC} as well as to GND are available as a stand alone function with the device name SN74ACT1071 and SN74ACT1073.



Floating bus lines normally occur only on bi-directional signal lines.

To avoid floating bus lines several actions can be implemented:

★ If the duration of the 3-state doesn't last longer than 5µs, the leakage currents can't charge the bus line into the threshold region.

★ With an intelligent bus protocol, long 3-state periods can be avoided. For example, the specification of the CPI bus states: The last user of the bus has to drive the bus with any valid logic level, until the next module requests and gets the bus. This is an intelligent solution with low power consumption.

★ Any resistor network at the line-end, like pull-up or pull-down resistors or any line termination, ensures defined logic levels during high impedance periods. This solution is not acceptable in low power environments.

★ Using bus-transceivers with integrated bus-hold cells or terminating the bus line by a bus hold circuit with integrated clamping diodes freezes the last active logic level. This is a good solution for low power systems.

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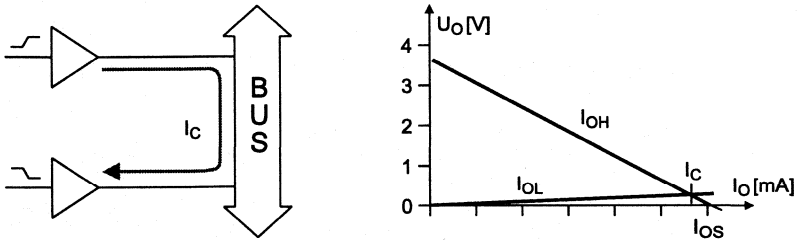
Bus Conflicts



★ **A bus conflict occurs when, from a timing mismatch, two line drivers apply different logic levels (voltages) to the bus at the same time.**

★ **The excessive output current I_O (≈ I_{OS}) causes high power dissipation, which results in a high chip temperature T_j.**

$$T_j = T_a + P_{TOT} * R_{\vartheta ja};\ (R_{\vartheta ja} = 80 \ldots 100°\ C/W)$$

Note: The chip temperature T_j must not exceed 150°C to avoid dramatic reliability degradation (mechanical stress, etc.).

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A bus conflict occurs when, from a timing mismatch, two line drivers apply different voltage levels to the bus at the same time. The excessive output current I_O (≈ I_{OS}) causes a high power dissipation, which yields in a high chip temperature T_j. According to the output characteristics, the output driving a high level is the "loser", but the designer can observe only a low level voltage a little bit higher than normal. In this situation the highest power dissipation can be observed in the output driving a high level, because this output has a voltage drop of $(V_{OH} - V_{OL})_{typ.} \approx 3V$ and the output current flowing is in the range of $I_{OS} > 100mA$.

To find out whether a reliability problem could arise or not, a examination of the overall power dissipation is necessary. With the overall power dissipation P_{TOT}, the ambient temperature T_a and the thermal resistance of the package $R_{\vartheta ja}$, the chip temperature T_j can be calculated with the following formula:

$$T_j = T_a + P_{TOT} \times R_{\vartheta ja};\ (R = 80 \ldots 100ºC/W)$$

The chip temperature T_j must not exceed 150°C. Otherwise there is a risk of dramatic reliability degradation because of mechanical stress between the silicon, the metal of the lead-frame and the plastic of the package.

Digital Design Seminar

Bus Conflicts

Calculation of the Power Dissipation of a Line Driver

$$P_{TOT} = P_Q + (P_S * t_s + P_O * 2t_p + P_C * t_C) * f * n$$

P_Q =	Quiescent power dissipation
P_S =	Average power dissipation caused by current spikes
t_s =	Duration of current spike
P_O =	Power dissipation caused by driving the transmission line
t_p =	Signal propagation time on the transmission line
P_C =	Power dissipation caused by the bus conflict
t_C =	Duration of the bus conflict
f =	Repetition rate
n =	Number of engaged outputs

The biggest contributors to power dissipation are :
1) P_Q 2) P_C 3) P_O

Therefore short bus conflicts (duration < 50 ns, Duty-Cycle < 10%) are mostly uncritical when using (A)LS, BiCMOS and CMOS circuits, but may be critical when using AS and F circuits.

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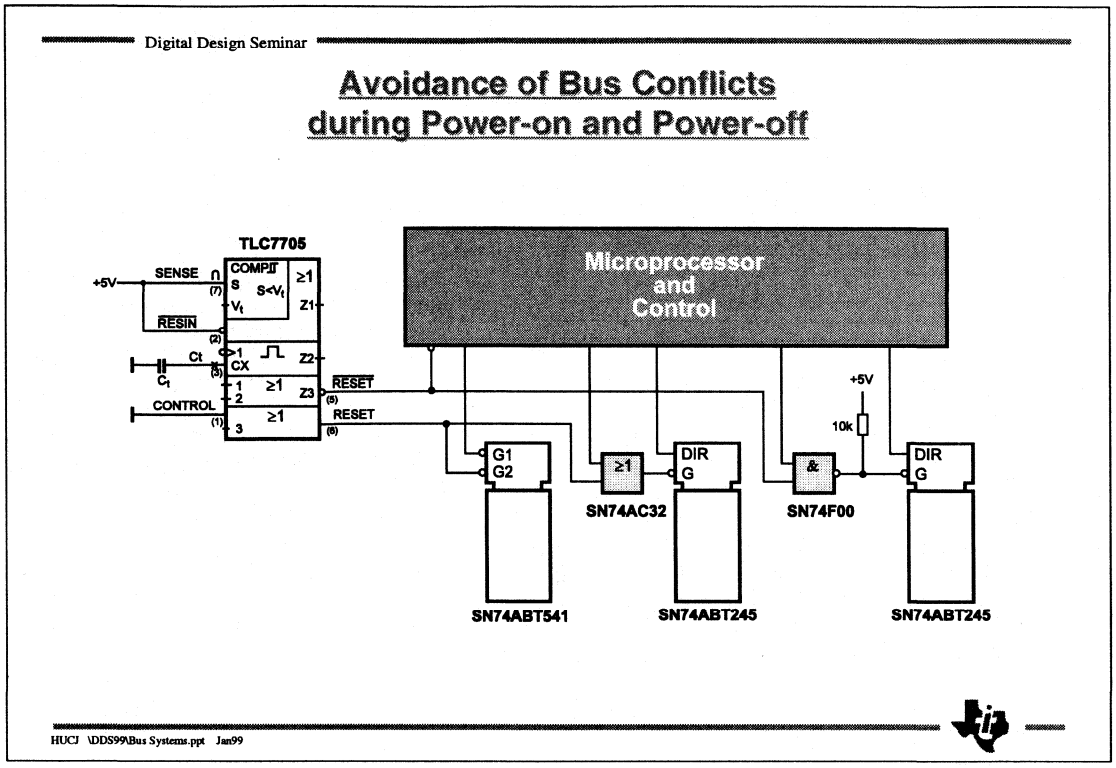
To calculate the overall power dissipation, not only the power dissipation of the bus conflicts (P_C x t_C) have to be taken into account, but also all the other sources like the quiescent power dissipation P_Q, the average power dissipation caused by the current spikes (P_S x t_S) and the power dissipation caused by driving output loads (e.g. transmission line) P_O.

Under typical conditions, bus conflicts that are shorter than 50ns with a duty-cycle of less that 10% are mostly uncritical when using LS, ALS, BiCMOS and CMOS circuits. It may be critical for AS or F circuits.



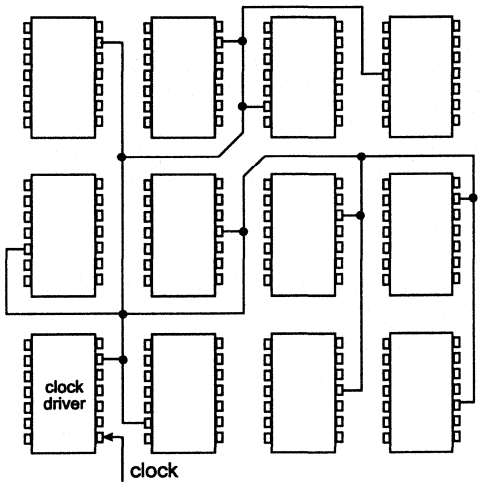
Bus conflicts don't occur only during normal operation. A good chance to generate bus conflicts for a long time is during power up and power down. Power supplies typically have settling times up to 100ms, while soft-start power supplies may even need more time to reach the final voltage. During the V_{CC} ramp-up, the different circuits start to work at different voltage levels and under worse case the bus drivers are already functional while the control logic connected to the "direction" and "enable" pins is still out of order. Under these circumstances very long bus-conflicts can occur, and especially when using widebus devices this often leads to destroyed devices.

Using bus functions with two enable inputs allows us to connect one of these enable inputs to the system-reset line. In this case the bus drivers are in high impedance during the reset period and when using a supply voltage supervisor like the TLC7705 this reset signal is active during power-up and power down. Drivers with only one enable input can be expanded to two inputs using external gates.

Digital Design Seminar

Clock Distribution

Digital: Bad distribution of the Clock Signals



- When drawing signal lines at random, each junction and line-end causes a point of discontinuity generating line reflections.
- The signal is heavily distorted. Malfunction of the system is probable.

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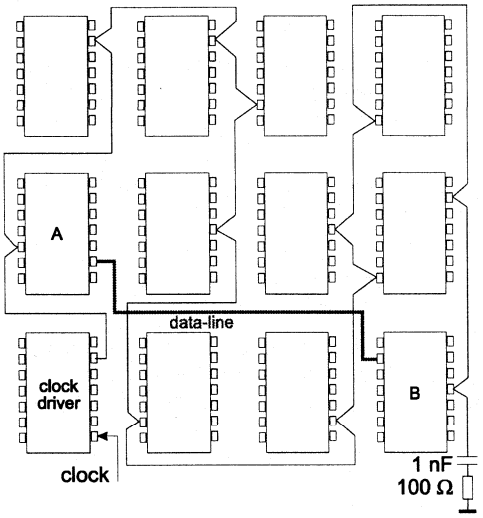
Another issue in all synchronous systems such as bus systems is the clock distribution network. The clock signal is the most important signal in every synchronous system because it is the signal with the highest frequency and has to be routed to nearly every chip within the system. Clean clock signal slopes are essential.

Under these circumstances the clock distribution network in the figure above is a bad example. According to transmission line theory signal reflections occur at every branch of the wiring and a bad wave form will be the result. Because of this the above example can't even be used for slow systems.

Digital Design Seminar

Clock Distribution

Digital: Right Clock Signal Distribution



- Interconnecting the circuits in series provides a homogeneous line impedance (in ECL systems the interconnections between the various circuits are all made the same length to ensure constant impedance along the line.
- Line termination eliminates reflections.
- Termination impedance 1...2 x Z_0.
- Typ. Propagation time: 10...20 ns/m.
- Note: Take care of interconnect propagation time.
- Be careful with data-lines: watch for "Race Condition"

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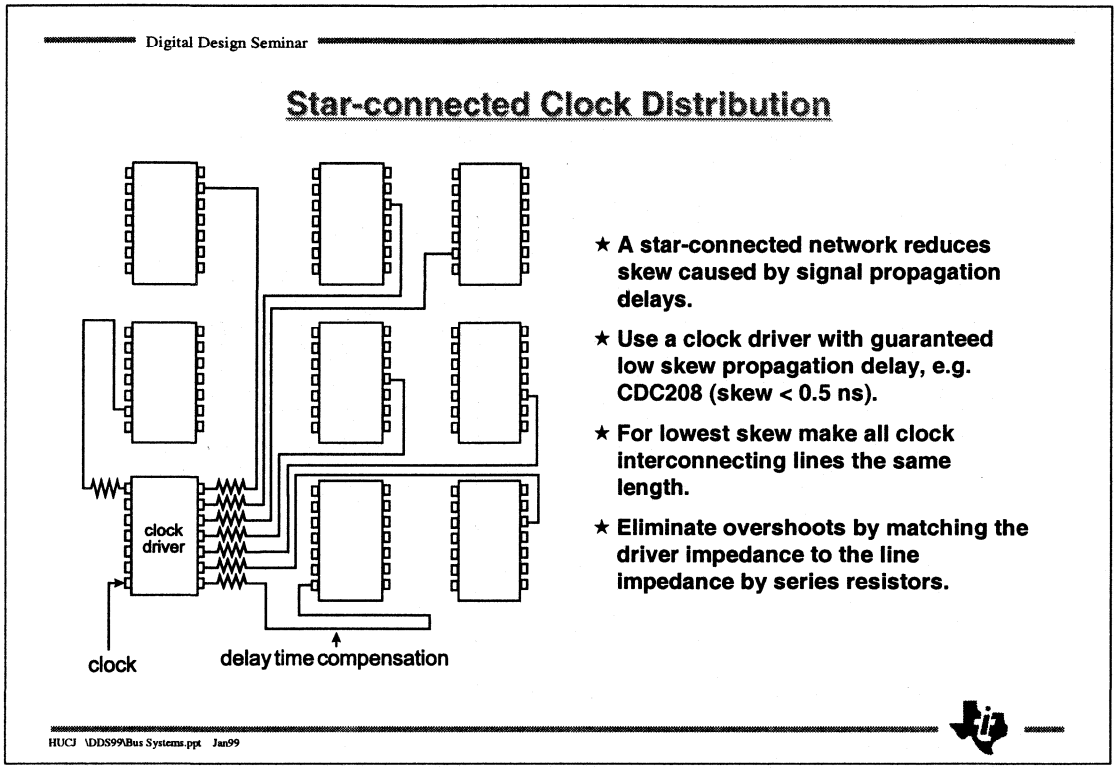
The minimum requirement for a clock distribution network is to use signal lines with a defined beginning and defined end-point and without any branches. In this case we can implement parallel line termination to guarantee excellent signal quality all along the signal trace. The above example is a solution mostly for slower systems, because the propagation delay time of the clock-signal along the clock-trace leads to a enormous skew: The slope arrives at different moment at the various clock inputs.

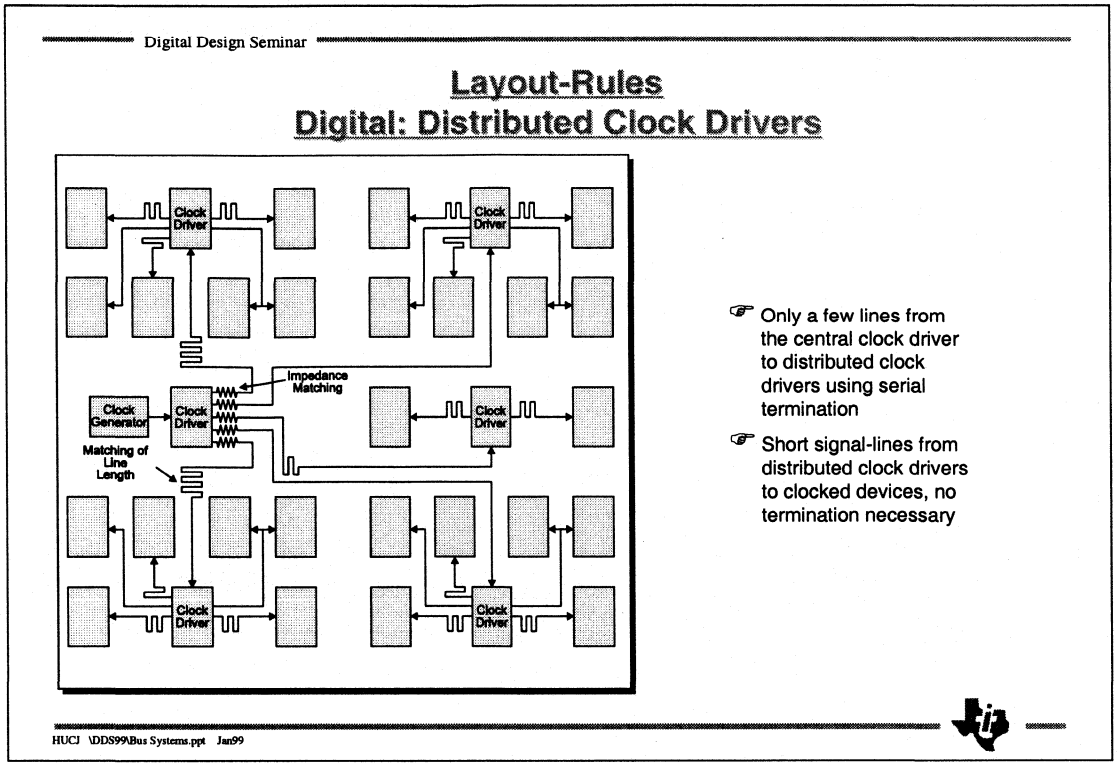
A special trap for designers is the "race condition". In above example a data-line carries a signal from device A to device B. While new data is generated in A, and the new data-signal runs to device B along the data-line, the clock signal has to go a long way from the clock input of device A to the clock input of device B. If the data-signal arrives at device B before the clock-signal, then the new data is clocked into device B using the same slope that has generated this data. This is not what the designer usually expects and malfunction of the complete system will be the result.



In most cases a star connected clock distribution network is the best solution for fast systems. To minimize the skew of the wiring the designer can chose equal length for all clock wires. Serial termination is the first choice for this lay-out, because these wires are point-to-point connections, which means that one output located at one end of the line drives one (or several) output(s) at the other end (or close to the other end) of the line.

If the board layout of the clock distribution network is made perfectly, the drivers of the clock signals should have the lowest skew possible. In this case the output skew is defined to be the difference in the propagation delay time between the slowest and the fastest driver within one clock driver package.

Texas Instruments offers a broad range of clock distribution circuits (CDC) that have guaranteed output skew values below 500ps.



In large electronic systems with a huge number of clock inputs the clock distribution network can be designed like a tree. The above example shows one primary clock driver whose input is connected to the clock generator and whose five outputs feed the inputs of five secondary clock drivers. The signal traces between the primary and the five secondary clock drivers are point-to-point connections and should be serially terminated. If the length of the traces between the five secondary clock drivers and the clock inputs of the clocked circuits are short enough, no termination is necessary.

To calculate the overall skew of this clock distribution network another skew definition is necessary: the process skew. This type of skew ($t_{sk(pr)typ.}$ < 1ns) guarantees a maximum difference in the propagation delay time between the fastest and the slowest driver in different packages. In above example the overall skew can be calculated in the following manner:

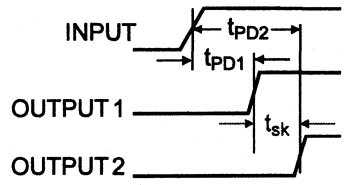
$$t_{sk(overall)} = t_{sk(0)} + t_{sk(pr)};$$

with $t_{sk(0)}$ = output skew of the primary clock driver

$t_{sk(pr)}$ = process skew of the five secondary clock drivers

Digital Design Seminar

Low-Skew Clock Driver



Output Skew
Skew between outputs of one circuit: $t_{sk(o)} \approx 0.5$ ns,

Process Skew
Skew between outputs of various circuits of same type $t_{sk(pr)} \approx 1.0$ ns,

Pulse Skew
Skew between rising and falling edge of outputs of one circuit: $t_{sk(p)} \approx 0.8$ ns,

CLOCK LINE BUFFERS	Input		output		Vcc
CDC111	1	PECL	9	PECL	3.3 V
CDC208	2	CMOS	8	CMOS	5 V
CDC316	1	TTL	18	TTL	3.3 V
CDC319	1	TTL	10	TTL	3.3 V
CDC328A	1	TTL	6	TTL	5 V
CDC329A	1	TTL	6	CMOS	5 V
CDC340, CDC341	1	TTL	8	TTL	3.3 V
CDC351/2351	1	TTL	10	TTL	3.3 V
CDC391	1	TTL	6	TTL	5 V
CDC392	1	TTL	6	CMOS	5 V

CLOCK LINE DRIVERS WITH DIVIDERS	Input		output		Vcc
CDC303	1	TTL	8	TTL	5 V
CDC337	1	TTL	8	CMOS	5 V
CDC339	1	TTL	8	TTL	5 V

CLOCK LINE DRIVERS WITH PLL	Input		output		Vcc
CDC509/2509	1	TTL	9	TTL	3.3 V
CDC2510	1	TTL	16	TTL	3.3 V
CDC516/2516	1	TTL	10	TTL	3.3 V
CDC536/2536	1	TTL	6	TTL	3.3 V
CDC582/2582	1	LVPECL	12	TTL	3.3 V
CDC586/2586	1	TTL	12	TTL	3.3 V
CDC587/2587	1	SSTL/TTL	16	TTL	3.3 V

CLOCK SYNTHESIZERS /DRIVERS	for PC Chipset
CDC9318, CDC9319	440BX
CDC913	
CDC9841, CDC9842, CDC9843	440TX

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Besides the output skew $t_{sk(0)}$ and the process skew $t_{sk(pr)}$ some clock drivers have a third type of skew: the pulse skew $t_{sk(p)}$. The pulse skew is defined as the maximum difference in propagation delay time between the rising and the falling edge of a clock signal. If it is necessary to guarantee a maximum duty cycle (e.g. 45%) for the clock signal, devices with a specified pulse skew should be chosen.

Texas Instruments offers a broad range of clock distribution circuit (CDC) with various functionalities:

★ single drivers and several drivers connected to one clock input

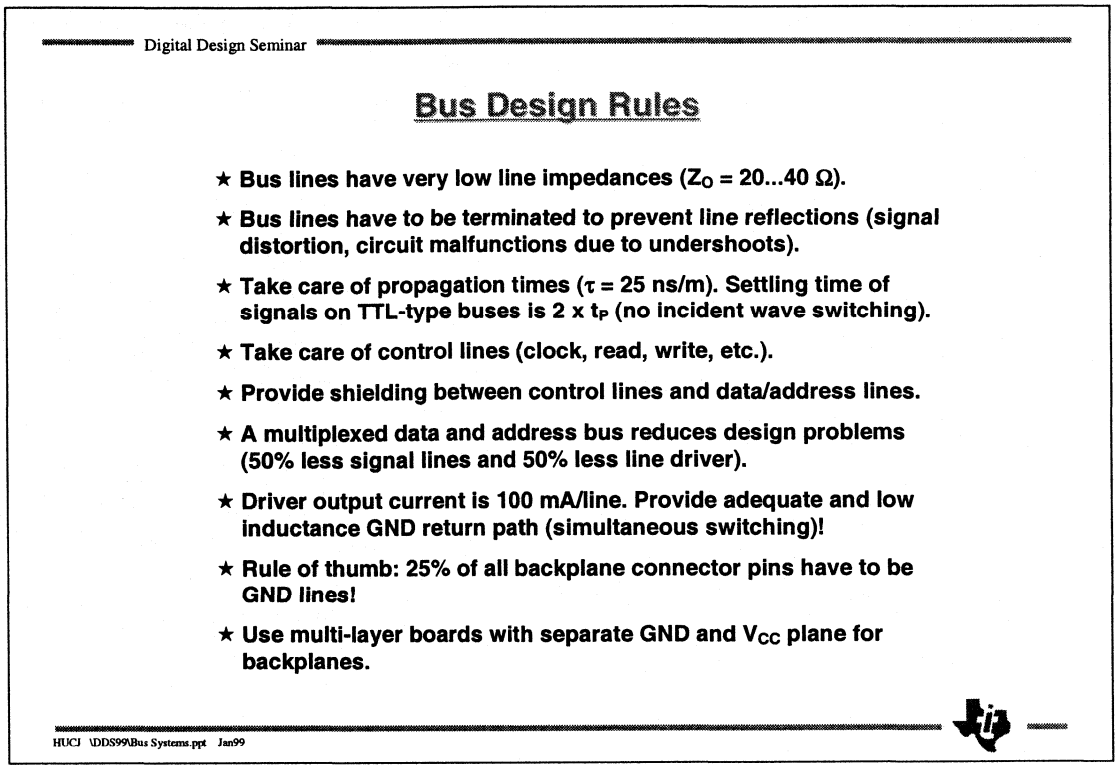
★ inverting and non-inverting types

★ with and without built in dividers

★ supply voltage V_{CC} = 5V and V_{CC} = 3.3V

★ clock drivers with and without PLL

★ application-specific clock drivers e.g. for PC motherboards

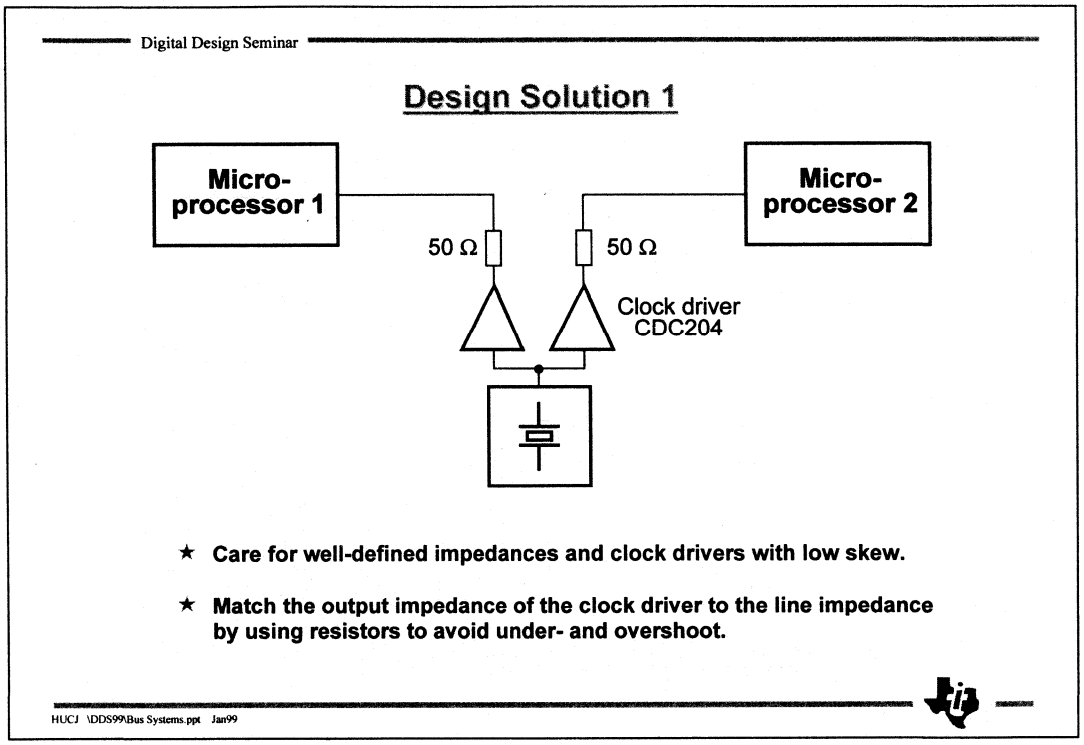


The above list shows a collection of bus design rules. Most of them have been already explained in detail on the previous pages.

One basic rule, not previously discussed. is the rule of thumb:

25% of all backplane connector pins have to be GND lines!

This huge number of GND pins is necessary to generate a low impedance and low inductance connection between the backplane and the modules. Otherwise it is not possible to get the necessary current, especially the peak values during current spikes, onto the modules. The GND lines should be distributed on the connector and not lumped together at one end (e.g. the bottom 3 rows). Otherwise the current path on the GND lines is too long from the backplane board to every location on the module and EMC problems can arise.

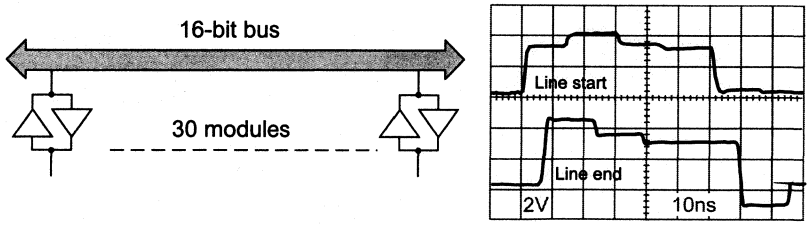


"Design Problem 1" had a bad clock distribution network. The clock driver was sitting close to microprocessor 1 and far away from processor 2. No line termination was included and therefore bad signal quality, caused by line reflections, was the result.

A clock distribution network in star connection with correct line termination leads to a reliable system.

Digital Design Seminar

Design Solution 2



★ **Signal integrity is now guaranteed by Incident Wave Switching.**

★ **System power dissipation is greatly reduced :**

2 x ABT25245 transmitter	**I_{CC} = 20.5 mA**
2 x ABT25245 receiver	**I_{CC} = 20.5 mA**
56 x ABT25245 3-state	**I_{CC} = 28.0 mA**
total	**I_{CC} = 69.0 mA *)**

*) Additional power consumption will be caused by required low impedance termination.
Recommended 60Ω 80Ω split termination on both line ends.

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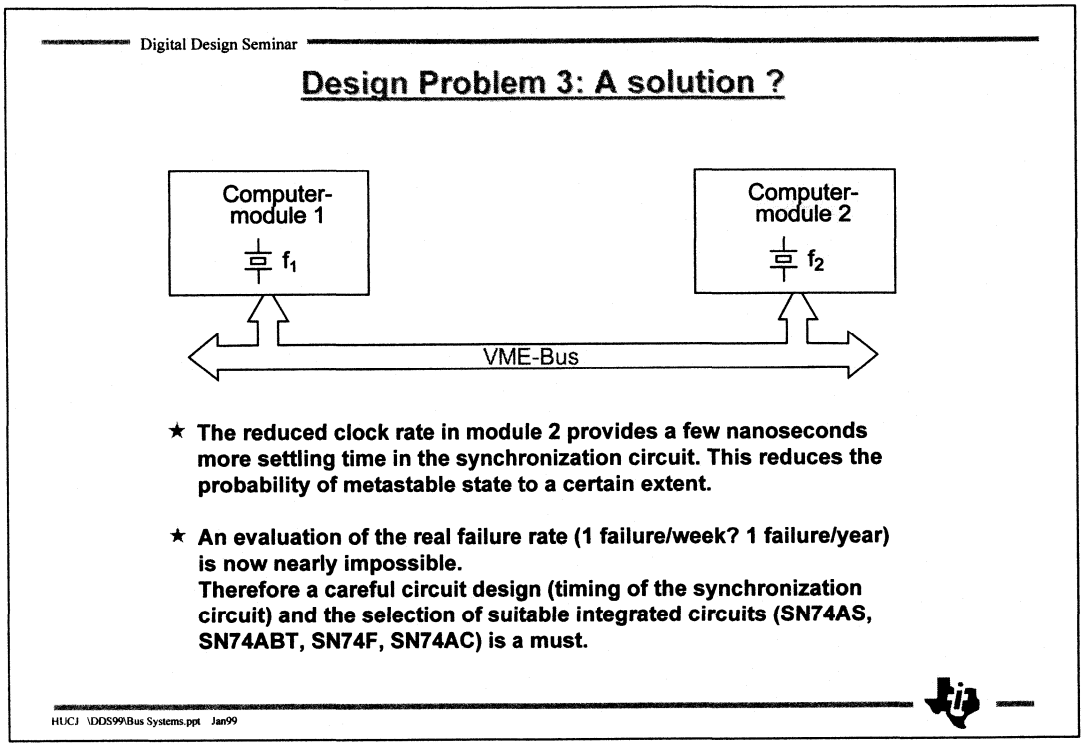
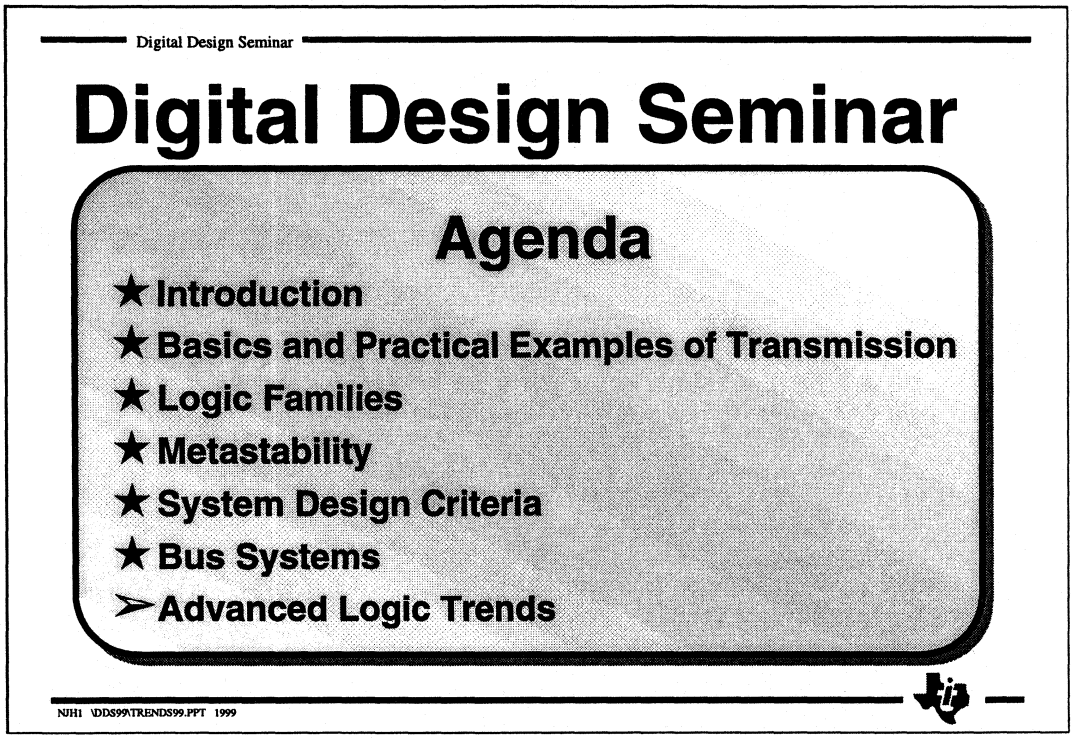
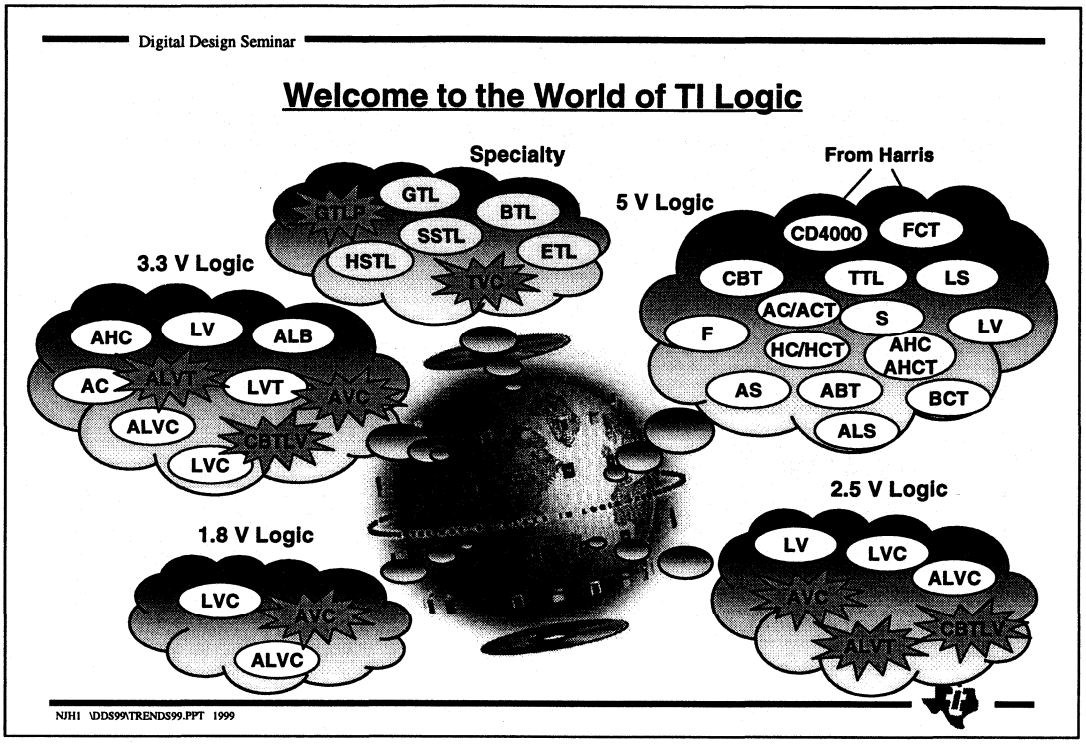
The designer of the backplane bus in "Design Problem 2" should have a closer look to the family of incident wave switching (IWS) driver SN74ABT25xxx. These drivers are able to switch the bus with the incident wave, so the signal quality on the backplane will be excellent. In addition, the current consumption of the drivers connected to the bus will drop from 6.5A down to 69mA!



The synchronization circuit of computer module 2 in the "Design Problem 3" had a mean time between failure (MTBF) rate less than one week. The reduced clock frequency of computer 2 increased the MTBF rate, but the designer didn't really know the actual value of his design (1 failure/week? 1 failure/year?). Therefore a careful circuit design (timing of the synchronization circuit, dual-rank synchronizer) and the selection of suitable integrated circuits (SN74AS, SN74ABT, SN74F, SN74AC) is essential to increase the MTBF rate into an uncritical region (e.g. 1000 years).


Digital Design Seminar
Digital Design Seminar
Agenda
★ Introduction
★ Basics and Practical Examples of Transmission
★ Logic Families
★ Metastability
★ System Design Criteria
★ Bus Systems
➢ Advanced Logic Trends
NJH1 \DDS99\TRENDS99.PPT 1999


Digital Design Seminar
Welcome to the World of TI Logic
Specialty
GTL
GTLP
BTL
SSTL
HSTL
ETL
TVC
From Harris
5 V Logic
CD4000
FCT
CBT
TTL
LS
AC/ACT
S
LV
F
HC/HCT
AHC
AHCT
AS
ABT
BCT
ALS
3.3 V Logic
AHC
LV
ALB
AC
ALVT
LVT
AVC
ALVC
CBTLV
LVC
2.5 V Logic
LV
LVC
ALVC
AVC
CBTLV
ALVT
1.8 V Logic
LVC
AVC
ALVC
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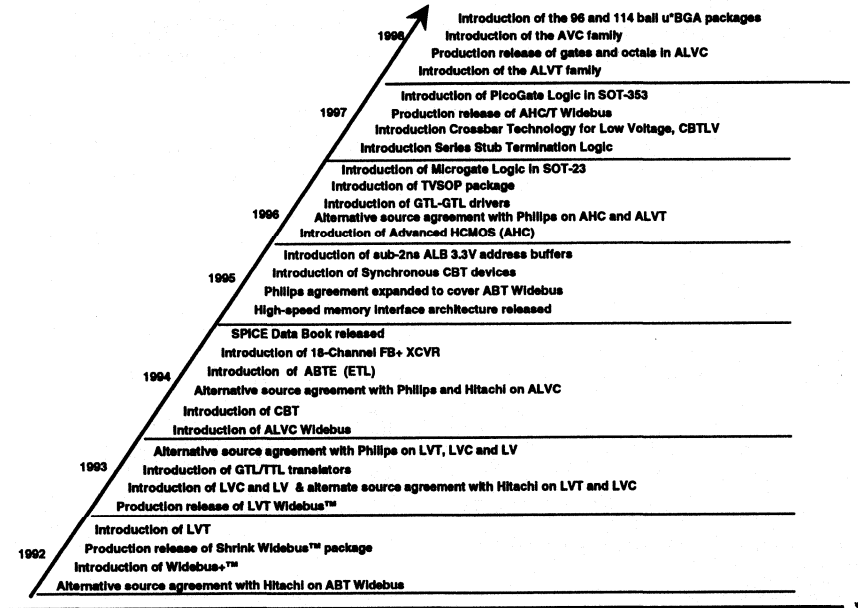
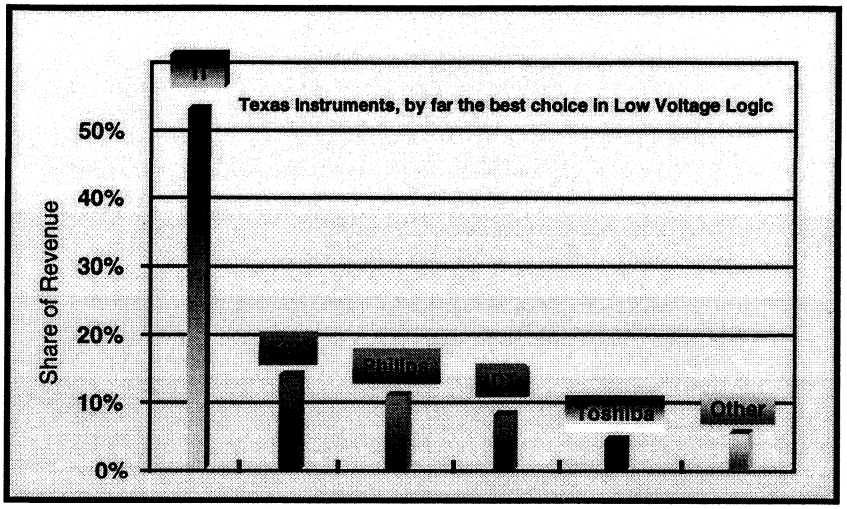
Industry Leading Logic Solutions From TI



Digital Design Seminar

Low Voltage Logic - 1997 Worldwide Market Share



Source: Insight Onsite May 1998
Chapter 1 Page 10

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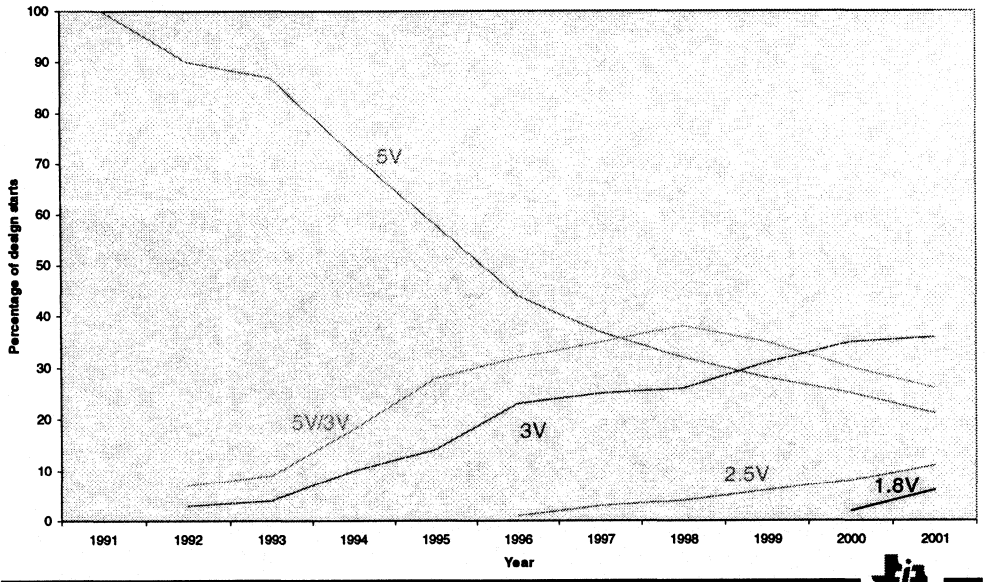
Moving to Low-Voltage Designs



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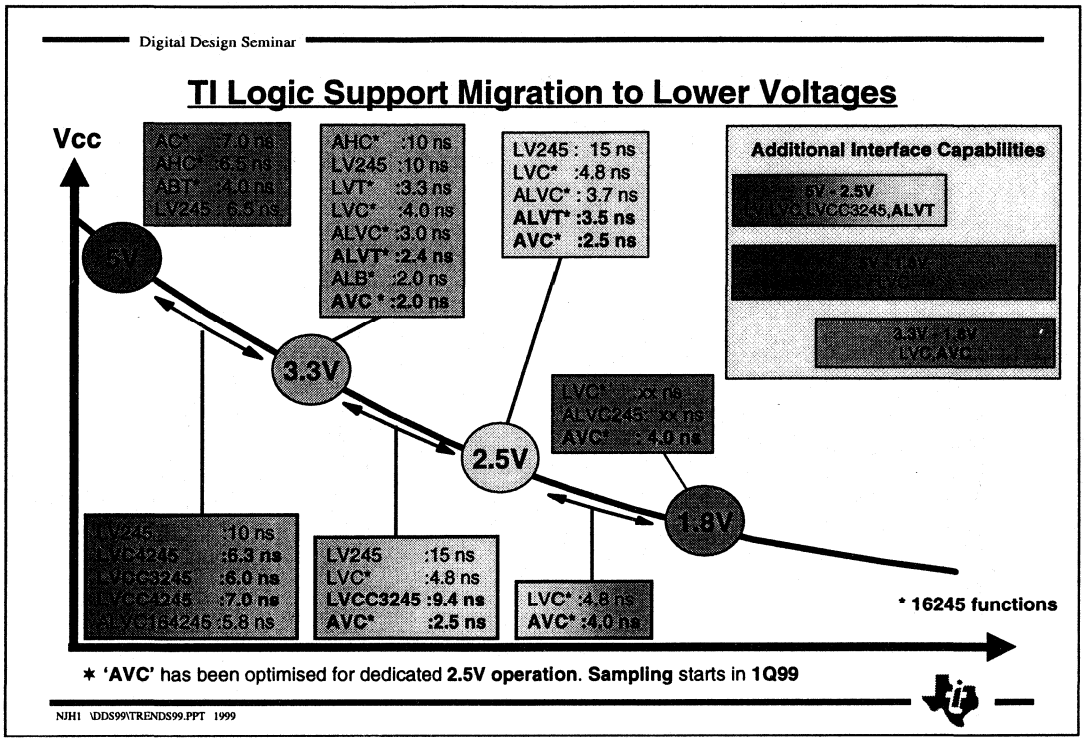
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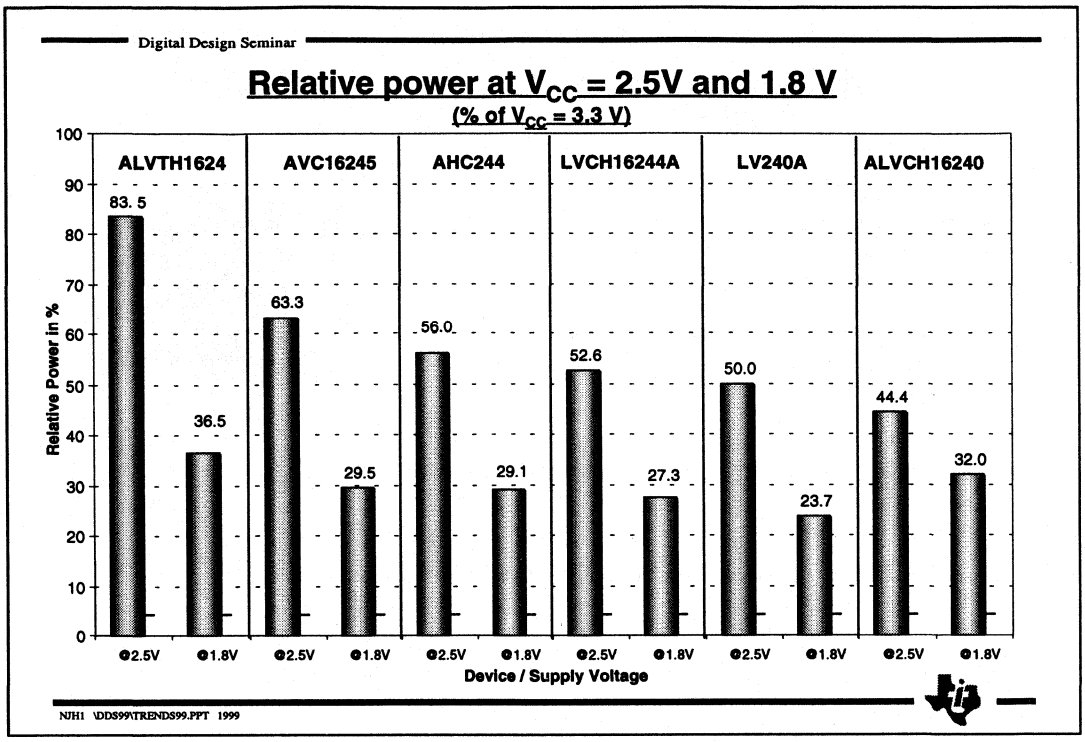
TI Logic Support Migration to Lower Voltages
Vcc
AC* :7.0 ns
AHC* :6.5 ns
ABT* :4.0 ns
LV245 : 6.3 ns
5V
AHC* :10 ns
LV245 :10 ns
LVT* :3.3 ns
LVC* :4.0 ns
ALVC* :3.0 ns
ALVT* :2.4 ns
ALB* :2.0 ns
AVC * :2.0 ns
3.3V
LV245 : 15 ns
LVC* :4.8 ns
ALVC* : 3.7 ns
ALVT* :3.5 ns
AVC* :2.5 ns
2.5V
LVC* :xx ns
ALVC245 : xx ns
AVC* : 4.0 ns
1.8V
LV245 :10 ns
LVC4245 :6.3 ns
LVCC3245 :6.0 ns
LVCC4245 :7.0 ns
LVC164245 :5.8 ns
LV245 :15 ns
LVC* :4.8 ns
LVCC3245 :9.4 ns
AVC* :2.5 ns
LVC* :4.8 ns
AVC* :4.0 ns
Additional Interface Capabilities
5V - 2.5V
LVC,LVCC3245,ALVT
3.3V - 1.8V
LVC,AVC
* 16245 functions
* 'AVC' has been optimised for dedicated 2.5V operation. Sampling starts in 1Q99
NJH1 \DDS99\TRENDS99.PPT 1999


Digital Design Seminar
Relative power at V_{CC} = 2.5V and 1.8 V
(% of V_{CC} = 3.3 V)
Relative Power in %
100
90
80
70
60
50
40
30
20
10
0
ALVTH1624
AVC16245
AHC244
LVCH16244A
LV240A
ALVCH16240
83. 5
36.5
63.3
29.5
56.0
29.1
52.6
27.3
50.0
23.7
44.4
32.0
@2.5V
@1.8V
Device / Supply Voltage
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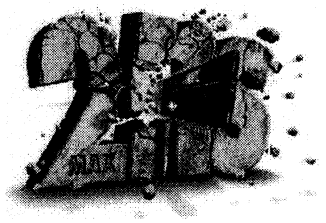
Advanced Very-Low-Voltage CMOS (AVC)

Fastest Logic Family Available - Sub 2 ns t_{pd}

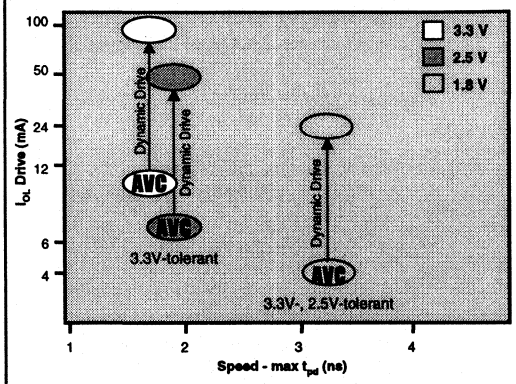


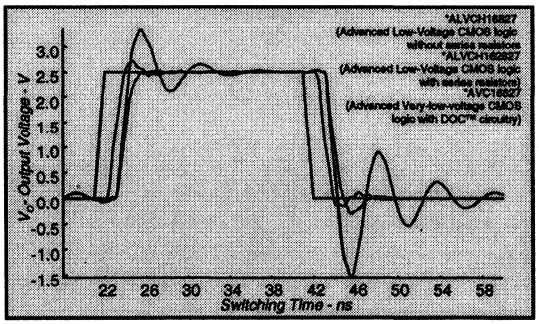
- **AVC is the industry's fastest low-voltage logic family**
  - <2ns maximum propagation delays at 2.5V
  - >40% faster than comparable devices
- **AVC features special circuitry that improves designs**
  - patent-pending Dynamic Output Control (DOC™)
  - I_{OFF}
  - Bus Hold™
- **AVC is optimized for 2.5V and supports mixed-mode systems at 1.8V and 3.3V**
- **AVC family is available in multiple JEDEC-standard advanced packages**

Digital Design Seminar

Dynamic Output Control (DOC™)

DOC only uses high drive when needed (during transition)





*Outputs waveforms are taken driving a PC100 Network Load
V_{CC} = 2.5V
T_J = 40 °C
Single Bit Switching

The DOC™ Circuit :

Provides high drive current to achieve maximum speed

Reduces over and undershoot normally associated with fast edges

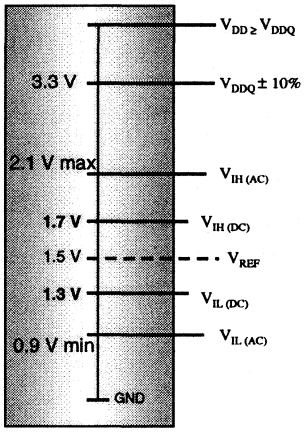
Eliminates need for damping resistors

Digital Design Seminar

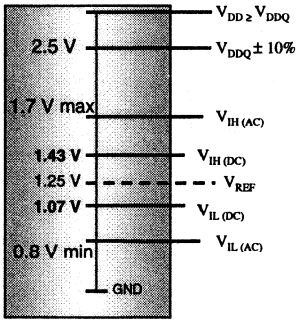
Series Stub Termination Logic (SSTL_3 / SSTL_2)

Next Generation SDRAM Memory Drivers

Level Specifications of SSTL_3



Level Specifications of SSTL_2



Description

- Supports **SSTL and LVTTL** signal inputs and outputs
- Drive = ± 20mA
- Interfaces with next generation SDRAMs
- Allows for point-to-point communication speed of 200 MHz

Available Devices

- SN74SSTL16837 : *20-bit SSTL_3 Universal Bus Driver*
- SN74SSTL16847 : *20-bit SSTL_3 Interface buffer*
- SN74SSTL16857 : *14-bit SSTL_2 registered buffer*

Package

- 64-Pin TSSOP (DGG)

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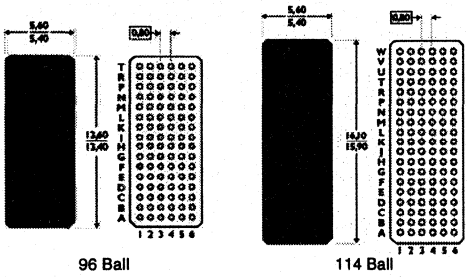
Digital Design Seminar

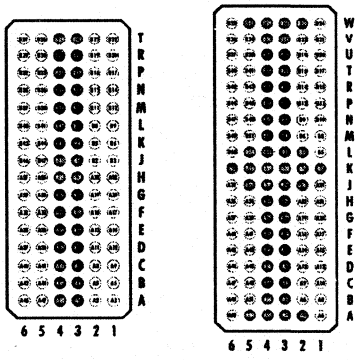
Low-Profile Fine-Pitch BGA Package

Package Dimensions



LFBGA Package Ball Out

- V_{CC}
- Ground
- Control / Ground / Data IN/OUT
- Data IN/OUT
- No Connect



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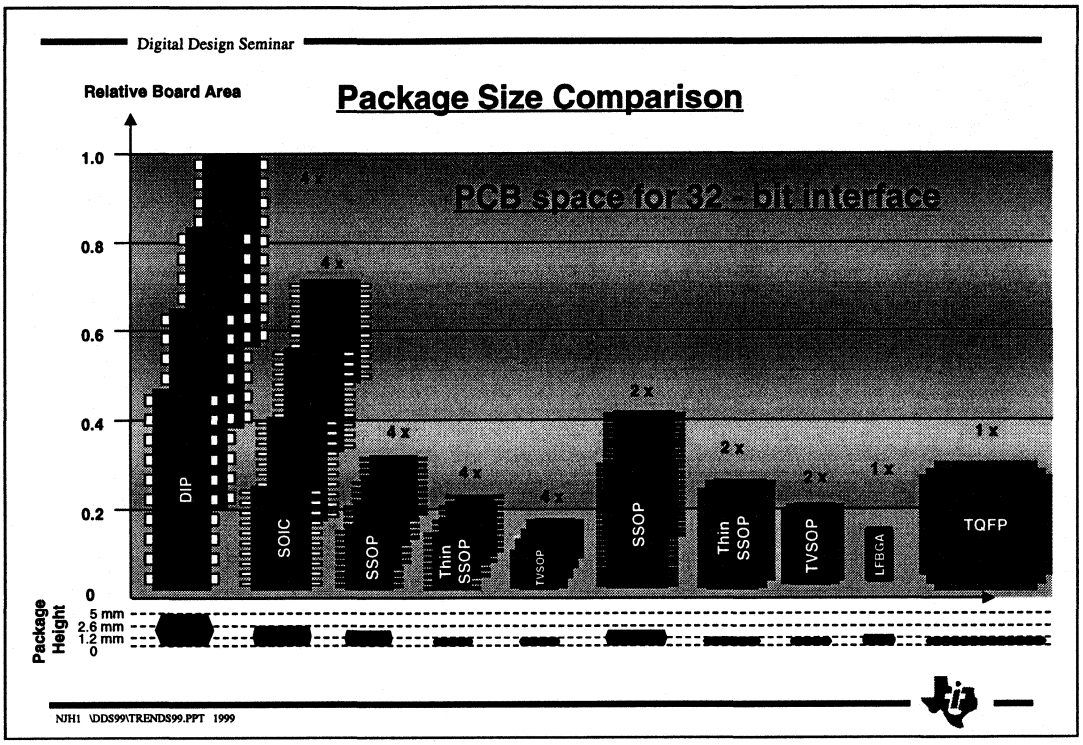
Digital Design Seminar
Relative Board Area
Package Size Comparison
PCB space for 32 - bit interface
1.0
0.8
0.6
0.4
0.2
0
4 x
4 x
4 x
4 x
4 x
2 x
2 x
2 x
1 x
1 x
DIP
SOIC
SSOP
Thin SSOP
TVSOP
SSOP
Thin SSOP
TVSOP
LFBGA
TQFP
Package Height
5 mm
2.6 mm
1.2 mm
0
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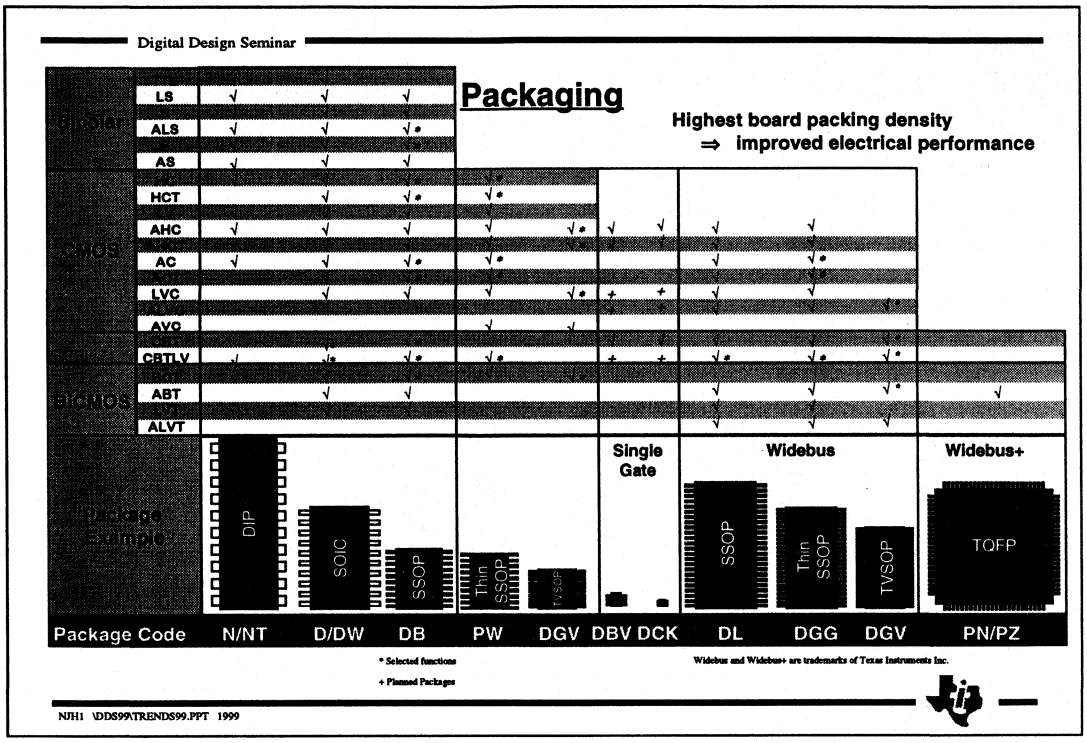
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Bipolar
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CMOS
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CBTLV
BiCMOS
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Package Example
DIP
SOIC
SSOP
Thin SSOP
TVSOP
Single Gate
SSOP
Thin SSOP
TVSOP
TQFP
Widebus
Widebus+
Package Code
N/NT
D/DW
DB
PW
DGV
DBV
DCK
DL
DGG
DGV
PN/PZ
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+ Planned Packages
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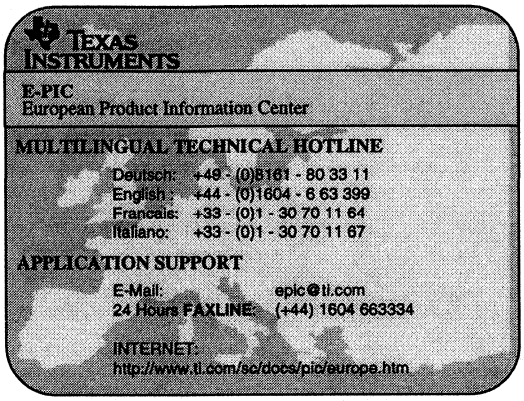
Texas Instruments Mixed Signal and Logic Literature

Listed below is a collection of Texas Instruments' Analog, Mixed Signal and Logic Products documentation. These documents can be ordered through a TI sales office, authorized distributor or the E-PIC (European Product Information Center) by referencing the literature code.

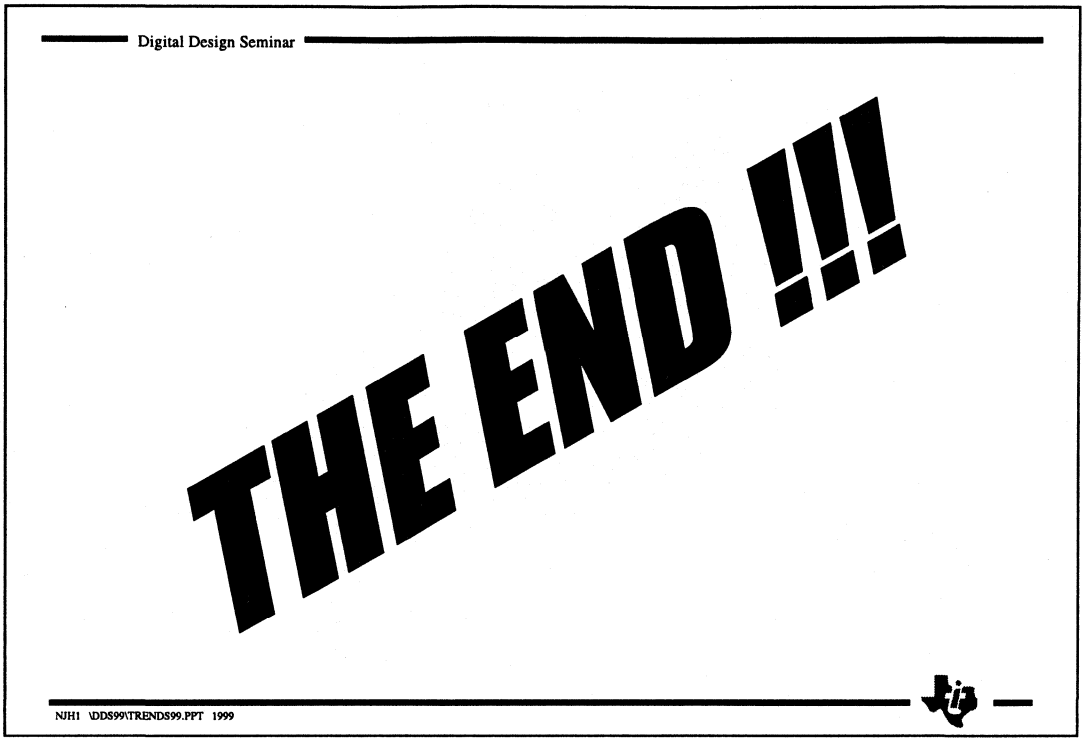
Analog and Mixed Signal	Revision	Lit-Code
Mixed Signal and Analog CD-ROM	1997	SLYC005A
Mixed Signal & Analog Designer's Guide	1997	SLYUE01A
Low-Voltage Analog and Mixed Signal Guide	1998	SLYBE03
Data Converter Selection Guide (Sine-On)	1998	SLAB035
Data Transmission Line Circuits Selection Guide	1997	SLLBE02A
Data Trans. Communication Controller Guide	1998	SLLBE03
Data Trans. High Speed Standards Guide	1997	SLLBE04
Audio Power Amplifier Guide (Sine-On)	1998	call E-PIC
Single Supply CMOS OpAmp Selection Guide	1996	SLOBE03
Rail-to-Rail OpAmp Selection Guide	1997	SLOBE02A
Excalibur OpAmp Selection Guide	1996	SLOBE01A
Low-Dropout Voltage Regulator Guide	1997	SLVBE01
TPIC Integrated Power Switches Selection Guide	1996	SLIBE01B
Data Acquisition Circuits Data Book	1998	SLAD001A
Data Transmission Line Circuits Data Book	1998	SLLD001B
Data Transmission Communication Controller	1996	SLLD003
IEEE1394 Solutions CD-ROM	1998	SLLC010A
Power Supply Circuits Data Book	1996	SLVD002
Operational Amplifier and Comparators / Vol. A	1997	SLYD011A
Operational Amplifier and Comparators / Vol. B	1997	SLYD012A
Data Transmission Design Seminar Manual	1998	SLLDE01C
Linear Design Seminar Manual	1998	SLYDE05

Logic	Revision	Lit-Code
Logic Selection Guide & Databook CD-ROM	1997	SCBC001A
Logic Selection Guide (First Half 1998)	1998	SDYU001J
Low Voltage Logic Selection Guide	1997	SCVBE01B
Microgate / PicoGate Logic Guide	1998	SCLT002
AHC Selection Guide	1997	SCLBE01B
AVC 2.5V Product Information	1998	SCEB003A
CBT Crossbar Switch Product Information	1998	SCDB002
GTL/ETL/BTL Backplane Selection Guide	1996	SCBBE04
GTL1655 Product Information	1998	SCET003
JTAG/Boundary Scan/IEEE1149.1 Guide	1998	call E-PIC
AHC/AHCT Data Book	1997	SCLD003A
AC/ACT Data Book	1996	SCADE02
ABT Data Book	1997	SCBD002C
LVT Data Book	1998	SCBD154
LVC,LV Data Book	1998	SCBD152A
ALVC Data Book	1997	SCED006
Widebus/Widebus+ Data Book	1995	SDWDE02
GTL,ETL,BTL Backplane Data Book	1995	SCBDE10
CBT Crossbar Switch Data Book	1996	SCDD001A
JTAG/Boundary Scan/IEEE1149.1 Data Book	1997	SCTD002A
Digital Design Seminar Manual	1998	SDYDE01B
Design Considerations for Logic Products	1998	SDYAE01

Contacts / Information



TI Home Page	http://www.ti.com
TI Logic Home Page	http://www.ti.com/sc/logic
TI Application Reports	http://www.ti.com/sc/docs/psheets/app_log.htm
TI Datasheets	http://www.ti.com/sc/docs/psheets/pids.htm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